A Dynamic Model and Control Strategy for the Combined Multipulse Multilevel Converter Based HVDC System

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Abstract

The multipulse multilevel converter topology is a newly introduced converter topology with the potential for high voltage direct current (HVDC) transmission applications. This paper focuses on harmonic reduction, control and design of multipulse multilevel converters for the realization of HVDC systems. Dynamic performance of the proposed converter based HVDC system with nominal power of 100 MW and voltage of 33 kV, 50 Hz is evaluated in the MATLAB/Simulink environment. The simulation results show that with the proposed converter topology and control strategy used, the HVDC station can respond satisfactorily to the system dynamics and control commands under steady state and dynamic load conditions while maintaining voltage balance of the DC capacitors.

Keywords : HVDC system, multipulse converter, multilevel inverter, total harmonic distortion, voltage source converter.

1. Introduction

The availability of high power, high frequency semiconductor switches with the gate turn off capability has made the implementation of high power voltage source converters (VSC) possible for utility applications including high voltage direct current (HVDC) systems [1-4]. The VSC based HVDC transmission system shown in Fig.1 has been widely accepted for either back-to-back or point-to-point bulk power transmission. The conventional 6-pulse converter suffers from relatively high input harmonic current when used as a rectifier and high output voltage harmonics when operated as an inverter. In response to the growing demands for high power converter units, multipulse converters (MPC) have drawn increased interest in the field of research and industry [5]–[8]. An MPC generates a waveform which closely resembles a sine wave by connecting a number of identical three-phase converter bridges through phase shifting transformers (PST). The key problem with multipulse converter is the requirement of magnetic interfaces constituted by complex zigzag phase shifting transformers which increases the cost of the complete system [5].

Recently, HVDC converter systems using full back-to-back multilevel diode-clamped converters are investigated, owing to their high-voltage, high-current and staircase-like waveform capabilities [9]. Hence an attractive alternative to the multipulse converter is the multilevel converter (MLC) [10]-[12]. In multilevel converters, a premium quality output waveform can be achieved with a sufficiently high number of voltage levels. However, the number of voltage levels is limited due to control complexity and cost. Additionally, a large number of DC capacitors

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are required. The voltages of these capacitors must be balanced in order to avoid over-voltages on any particular link. A critical review of literature shows neither multipulse converters nor multilevel converters are useful on their own. A hybrid converter topology incorporating the advantages of both MPC and MLC will be attractive [13].

The main objective of this paper is to develop a multipulse multilevel converter topology and to use it for the realization of a back-to-back connected HVDC system. The harmonic performance of this converter topology as rectifier for AC to DC conversion and as an a inverter for DC to AC conversion is evaluated through MATLAB based simulation. Addionally, the paper investigates the behaviour of the proposed HVDC system under comprehensive scenarios such as steady state conditions and dynamic conditions for converter stations operating with a single frequency and stations with different frequencies.

2. Converter station operating as a rectifier

The three phase fully controlled VSC shown in Fig. 2 has probably been the most widely used power electronic converter in the medium to high power applications. Fig. 3 shows the output voltage and the supply current waveform of a fully controlled 6 pulse rectifier. Although it is the simplest configuration, it suffers from a relatively high value of harmonic components in the input current which in turn amounts to the high value of total harmonic distortion (THD) of 30.69% as depicted in Fig.4.

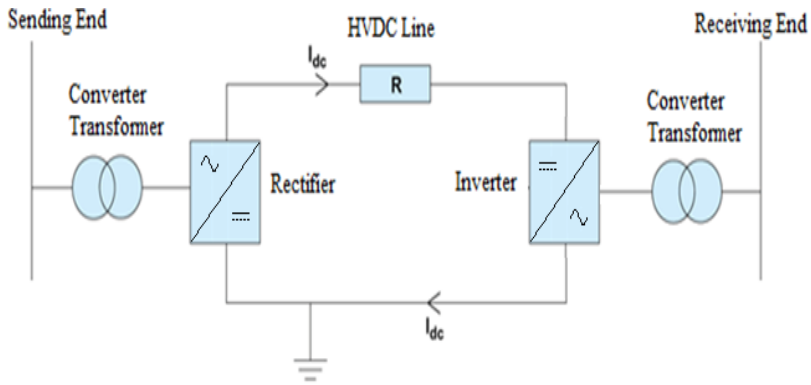

Fig .1. A Schematic diagram of an HVDC system.

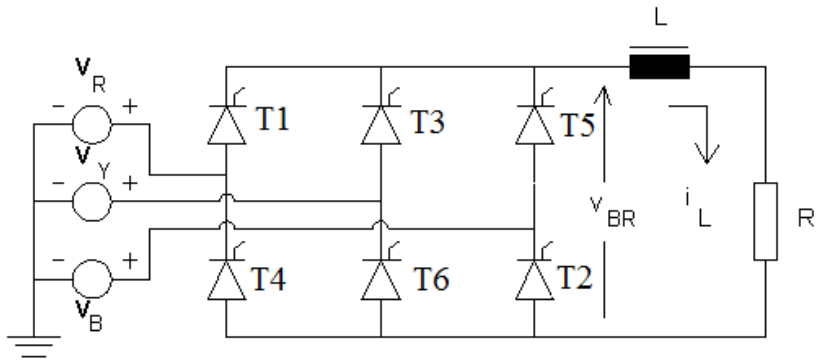

Fig .2. A fully controlled 6 pulse VSC**.**

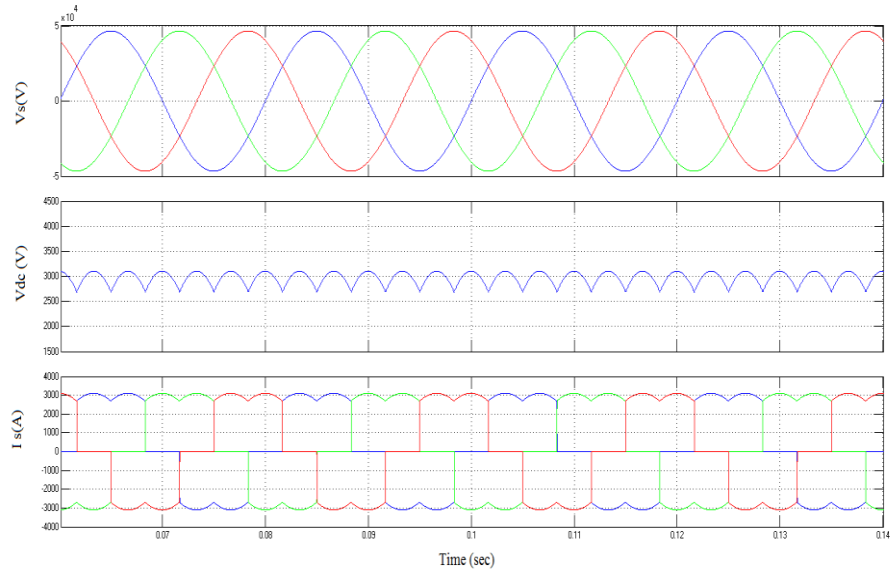

Fig.3. Output waveforms of a 6 pulse rectifier**.**

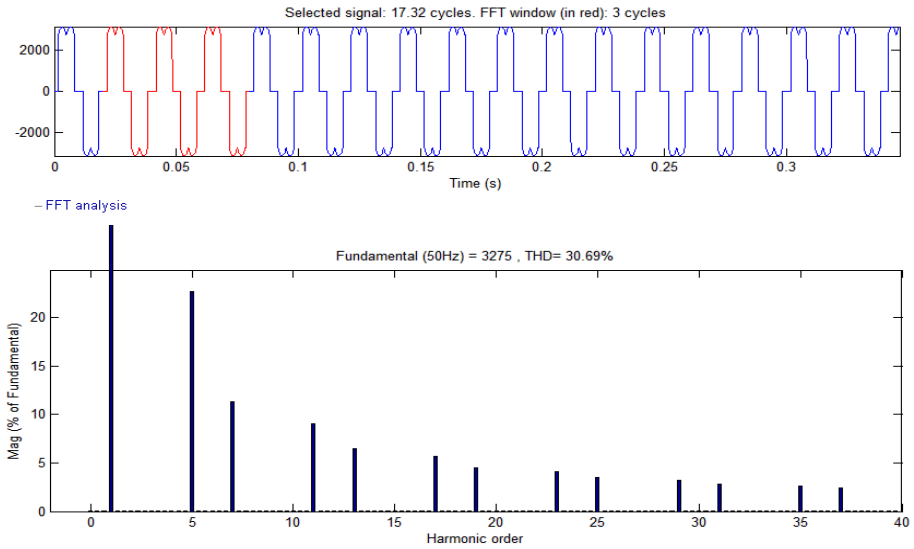

Fig. 4. The THD of supply current.

In order to overcome this drawback one of the solutions is to go for multipulse converters. For an n-pulse converter, the characteristic harmonics are of the order of **nk ± 1** where k = 1, 2, 3, …∞. The higher the pulse number, the lower the order of input current harmonics, lower the ripple content on the DC voltage and the higher the ripple frequency will be. Four basic 6-pulse converters as depicted in Fig.5 are connected in parallel with an appropriate phase shift to achieve a 24-pulse converter operation. The phase shift is designed so as to make the transformer construction identical. The transformer turns ratio is chosen according to the DC link voltage requirement. Fig.6 shows the transformer connections used to realize a 24-pulse voltage source converter. The phase displacement pattern is shown below in Table 1.A phase shift of ±7.5° is introduced by the phase shifting transformer in the input AC supply in order to have a phase shift of 15° between two adjacent converter inputs and the corresponding phase shift of ±7.5°, -22.5º and -37.5 º are introduced in the gating circuits of the 6 pulse converters.

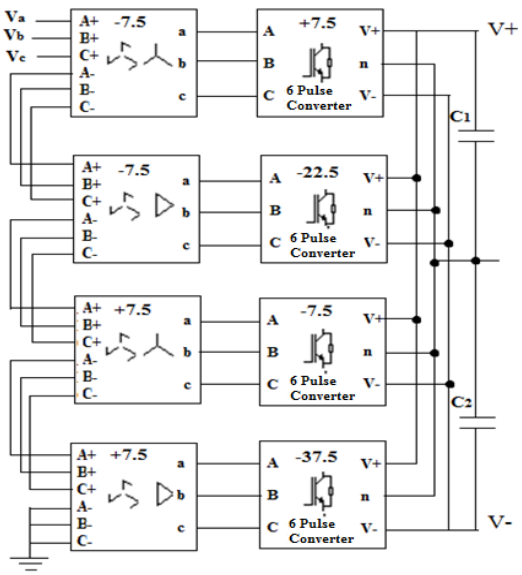

Fig .4. 24 Pulse converter operated as a rectifier**.**

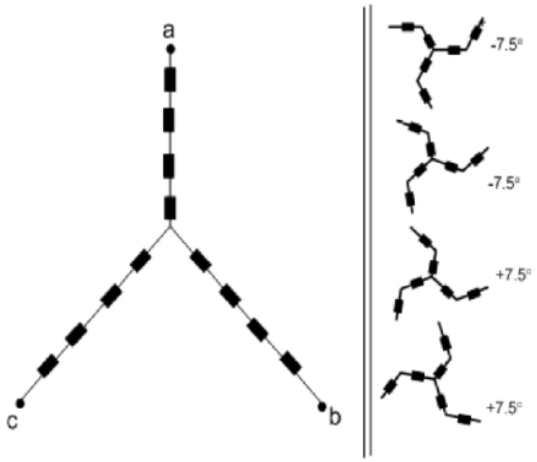

Fig .5. Transformer connections**.**

The 24 pulse DC output voltage resulting from the cascading of four fully controlled converters with an appropriate phase shift between them is shown in Fig.7. Furthermore, this figure depicts the elimination of lower order harmonics in the supply current resulting in a sinusoidal waveform. The lowest order harmonics present in the supply current are the 23rd and 25th.These values are typical of a 24- pulse system. This is highlighted in Fig. 8 and results in a total harmonic distortion of 1.1%. Thus, with a 24- pulse converter, the supply current THD is significantly reduced without any filtering equipment. The multiplication of the pulse number helps in the elimination of the input current harmonics and the reduction of ripple content in the DC link voltage. This ensures that the converter that has been developed could very well be employed for an efficient modeling of a HVDC system.

Table 1. Phase displacement pattern for a 24-pulse rectifier**.**

Coupling Transformer	Converter gate pulse	Phase shifting transformer
Y-Y	+7.5°	-7.5°
Δ-Y	-22.5°	-7.5°
Y-Y	-7.5°	+7.5°
Δ-Y	-37.5°	+7.5°

3. Converter station operating as an inverter

The 24- pulse inverter shown in Fig. 9 is obtained by combining four three-level diode clamped multilevel inverters with adequate phase shifts between them. The configuration of each three-level diode clamped multilevel inverter is shown in Fig.10. The voltages generated by each of the three level inverters are applied to the secondary windings of four different PSTs. Two of them are Y-Y transformers with a turns ratio of 1:1, and the remaining two are Δ-Y transformers with a turns ratio of 1:√3. The primary windings of the PSTs are connected in series, and the proper pulse pattern, which is the same as that tabulated in Table 1. is maintained so that the fundamental components of the individual 3-level inverters are added in phase on the primary side.

A. Selective Harmonic Cancellation

Fig.11 shows the conduction angle (σ) and the dead angle (β) in the output of a three-level diode clamped inverter. The operation of the three-level voltage source converter at different values of the dead angle (β) gives different harmonic performance [9]. Therefore, if this converter is employed to realize HVDC system, the power quality of the system can be enhanced by using three level voltage converters operating at an appropriate dead angle (β). The relationship between the conduction angle (σ) and the dead angle (β) is given as,

$$\sigma = 180° - 2\beta \tag{1}$$

The value of σ can be varied to minimise any particular harmonic component as,

$$\sigma = 180°\left(1 - \frac{1}{n}\right) \tag{2}$$

where n is the order of the harmonic that is to be minimized.

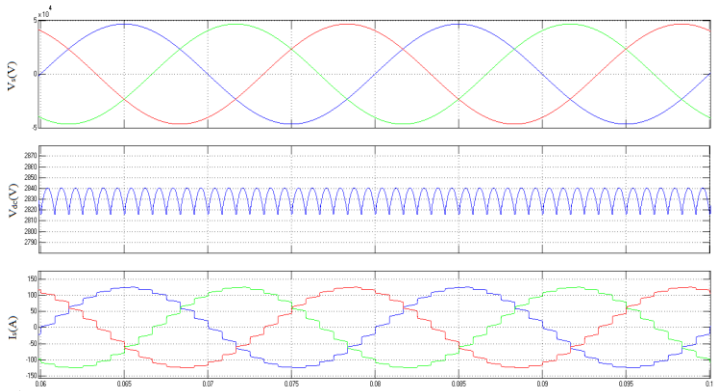

Fig .6. Output waveforms of 24-pulse rectifier**.**

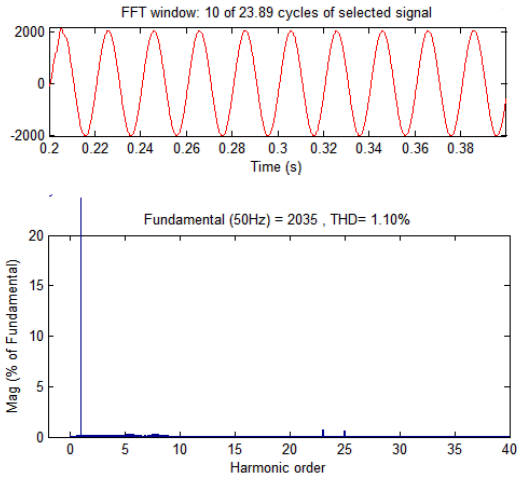

Fig .7. THD of the supply current**.**

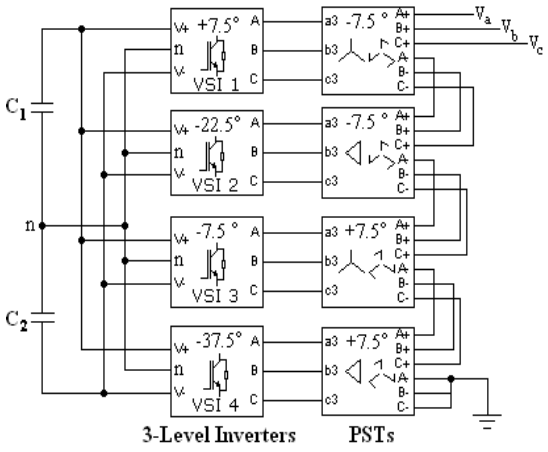

Fig .8. The combined multipulse-multilevel inverter.

In the 24-pulse converter, harmonics of the order 24k±1 (i.e. 23, 25, 47, 49….) are present. The minimum and dominant order harmonics are the 23rd and the 25th, and the conduction angle required to minimise these harmonics is σ = 172.17º, whereas the dead angle β is chosen as 3.9º. At these angles, not only the 23rd and 25th harmonics are eliminated, but other dominating harmonics are also minimised to a reasonable level leading to a sinusoidal AC output voltage as shown in Fig. 12. The THD plot shown in the Fig. 13 describes the presence of only the 47th and 49th harmonic components and the corresponding reduction in THD to 2.95%.

4. The proposed HVDC system

Fig.14 shows the circuit configuration of a proposed three-level, 24-pulse voltage source converters connected back to back to form the HVDC system. It consists of four three-level voltage source converter bridges at one side. All four converters are connected in parallel at the DC side with energy storing midpoint DC capacitors. The HVDC system is rated for 100 MW. Here the DC link voltage is chosen to be as low as 5 kV, which is most suitable for back-to-back HVDC system. A total of (4x12) 48 devices are used on each side of the converter system. The DC link voltage can be designed according to the converter system configuration. In the other side for DC to AC conversion, four identical 3-level diode clamped inverter configurations with a proper phase shift are considered, and their phase shifted AC output voltages are added in series on the primary windings of the transformer. Fig 14 shows the overall design of the HVDC system with the proposed 24-pulse converter operating as a rectifier on one side and as an inverter on the other side.

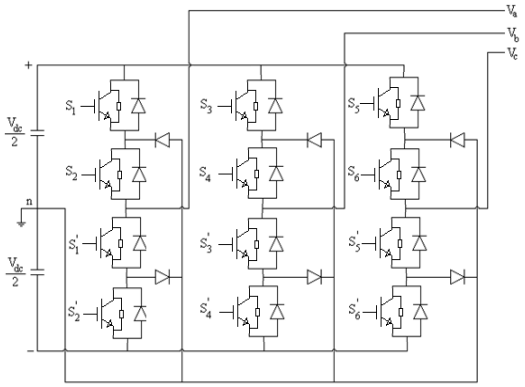

Fig .9. 3-level diode clamped inverter.

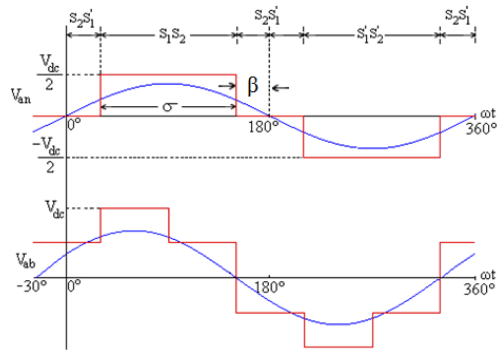

Fig .10. 3-level diode clamped inverter output voltage.

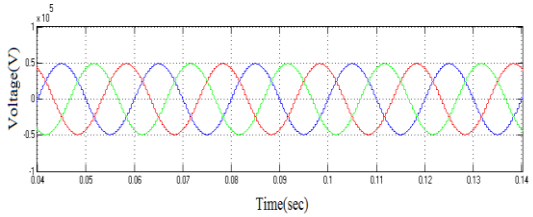

Fig .11. Output voltage of the 24-pulse inverter.

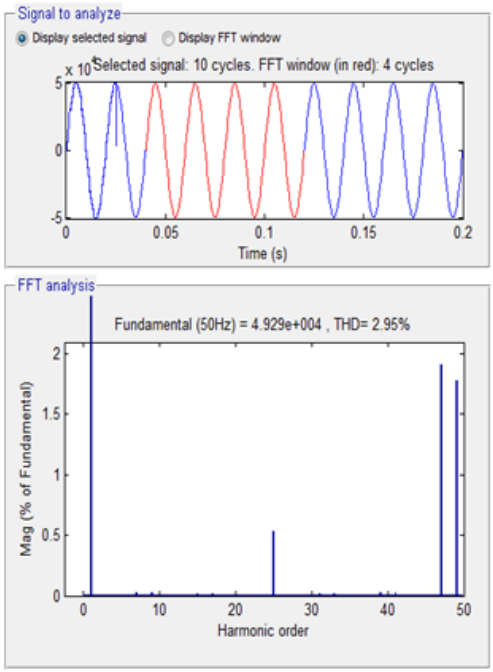

Fig .12. Output voltage THD.

5. Open loop operation

The proposed multipulse multilevel converter based HVDC transmission is realized in the MATLAB / Simulink environment, and the corresponding simulink model for open loop operation is shown in Fig. 15. The parameters used for the simulation are given in Table 2.

The HVDC transmission system consists of two stations. One station acts as a 24-pulse rectifier, and the other acts as a 24-pulse inverter. Thus, the AC voltage in station 1 is converted to DC through the rectifier. Power transmitted as DC power and the DC is converted to the required AC voltage of station 2 through the inverter. The waveforms of the converter station 1 voltages and currents, The DC link Voltage, the DC link current, the converter station2 voltages and currents are demonstrated in Fig. 16 for the load variations given at t=0.3s and t = 0.5s, respectively. Upon the addition of load, there is a dip in the DC voltage. As a consequence of this, the grid voltage decreases, an outcome which is not acceptable. For the above reasons, we choose closed loop control, ensuring that a constant DC voltage is maintained irrespective of the load variations.

6. Closed loop control

The coordinated control of two converter stations is the heart of the HVDC system for dynamic control of the active and reactive power. The closed loop control scheme is developed from a mathematical model of the VSC- HVDC system.

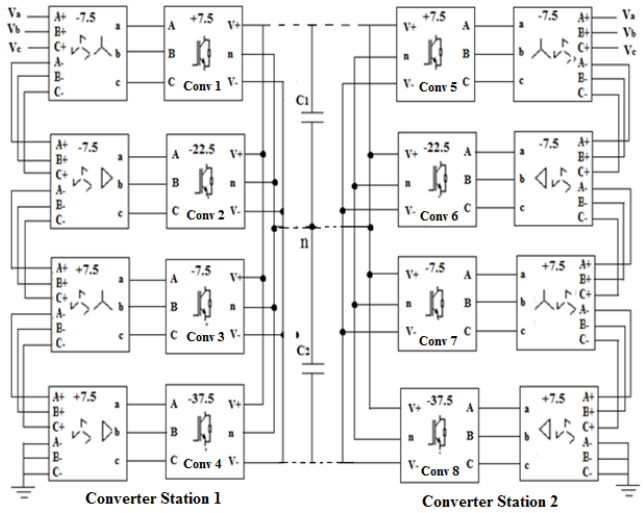

Fig .13. 24-pulse voltage source converter based HVDC system configuration.

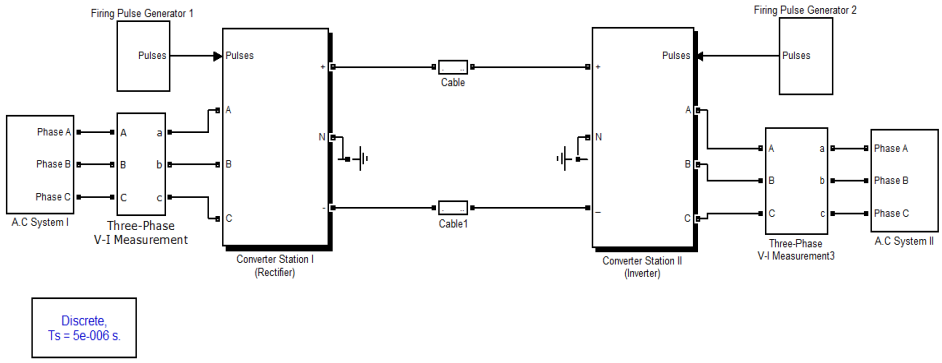

Fig .14. Open loop simulink model of HVDC system.

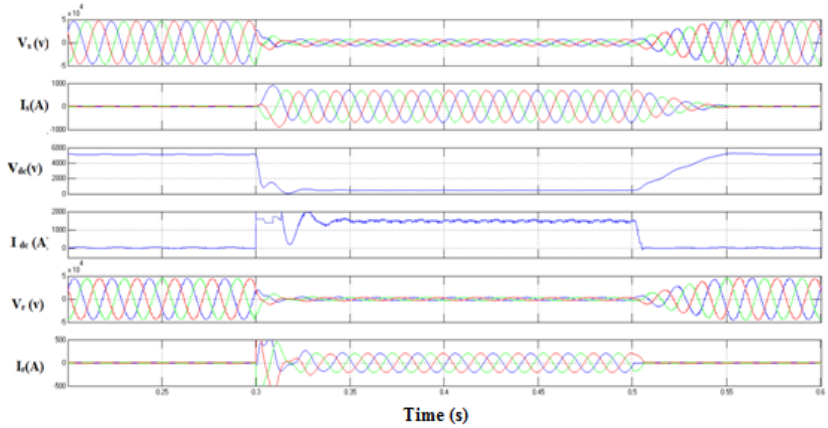

Fig .15. Waveforms for stations with the same frequency.

Table 2. Design Parameters.

Parameter	Symbol	Value
Rated active power	P	100MW
Supply voltage	V_s / V_r	33kV
Frequency	f_1 / f_2	50Hz / 50Hz
AC inductance	L1 / L2	6.9mH/ 6.9mH
DC link voltage	V_{dc}	5 kV
DC link capacitance	C_{dc}	0.125 mF
Resistance	R	0.015Ω/km
Transformer power rating	VI_t	100 MVA
Transformation Ratio	n	¼
Transformer Voltage	$V_{primary}$ / $V_{secondary}$	33 kV / 2.1kV
Transformer inductance	L	5mH

A. Dynamic Model of VSC-HVDC

The AC-to-DC 24-pulse converter model is depicted in Fig.17. The system consists of four 6-pulse converters. The DC-side of the 24-pulse converter is composed of two identical capacitors. All the losses in the 24-pulse converter and transformer are represented by an equivalent resistance R, while the transformer inductance is represented by an equivalent inductance L. For simplicity, the following assumptions are made:

1) The system parameters and the system voltages are three phase balanced.

2) The power switches, diodes and passive components of four 6-pulse converters are correspondingly identical.

The equations governing the instantaneous values of the three-phase voltages across the supply side of the rectifier and the current flowing into it are given by

$$\begin{pmatrix} \frac{di_{sa}}{dt} \\ \frac{di_{sb}}{dt} \\ \frac{di_{sc}}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-R}{L} & 0 & 0 \\ 0 & \frac{-R}{L} & 0 \\ 0 & 0 & \frac{-R}{L} \end{pmatrix} \begin{pmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{pmatrix} + \frac{1}{L} \begin{pmatrix} v_{ma} & -v_{sa} \\ v_{mb} & v_{sb} \\ v_{mc} & v_{sc} \end{pmatrix} \quad (3)$$

where i_s is the supply current

Since the system is assumed to be a balanced one, it can be transformed into a synchronous d- q-o frame by applying Park's transformation.

$$\begin{pmatrix} \frac{di_{sd}}{dt} \\ \frac{di_{sq}}{dt} \end{pmatrix} = \begin{pmatrix} \frac{R}{L} & \omega \\ -\omega & \frac{-R}{L} \end{pmatrix} \begin{pmatrix} i_{sd} \\ i_{sq} \end{pmatrix} + \frac{1}{L} \begin{pmatrix} v_{md} & -v_{sd} \\ v_{mq} & -v_{sq} \end{pmatrix} \quad (4)$$

where ω is the synchronous angular speed of the network voltage.The power balance equation between the dc and ac terminals of the converter is

$$P = V_{dc} I_{dc} = \frac{3}{2}\left(V_{sd} I_{sd} + V_{sq} I_{sq}\right) \quad (5)$$

Because of the 24-pulse configuration, all the harmonics produced in the supply current i_s of the converter are cancelled, and the equation relating the DC side and AC side can be written as

$$V_{sd} = kV_{dc} \cos\phi \quad (6)$$

$$V_{sq} = kV_{dc} \sin\phi \quad (7)$$

where $\phi = \tan^{-1}\left(\frac{V_{sq}}{V_{sd}}\right)$ is the angle between the converter voltage and the system voltage; k is the ratio between the AC and DC voltage of the inverter; and V_{dc} is the DC link voltage. Substituting V_{sd} and V_{sq} in equation (5), we obtain

$$\begin{aligned} I_{dc} &= \frac{3k}{2}\left(I_{sd}\cos\phi + I_{sq}\sin\phi\right) \\ &= C_{dc}\frac{dv_{dc}}{dt} = \frac{3}{2}\left(kV_{dc}\cos\phi I_{sd} + kV_{dc}\sin\phi I_{sd}\right) \end{aligned} \quad (8)$$

$$\frac{dv_{dc}}{dt} = \frac{3k}{2c_{dc}}\left(kV_{dc}\cos\phi\, I_{sd} + kV_{dc}\sin\phi\, I_{sd}\right) \quad (9)$$

With equations (4) and (9), the complete system equation could be expressed in a matrix form as given in equation (10):

$$\begin{pmatrix} \frac{di_{sd}}{dt} \\ \frac{di_{sq}}{dt} \\ \frac{dv_{dc}}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-R}{L} & \omega & \frac{k}{L}\cos\phi \\ \omega & \frac{-R}{L} & \frac{k}{L}\sin\phi \\ \frac{3k}{2c_{dc}}\cos\phi & \frac{3k}{2c_{dc}}\sin\phi & 0 \end{pmatrix} \begin{pmatrix} i_{sd} \\ i_{sq} \\ v_{dc} \end{pmatrix} + \frac{1}{L}\begin{pmatrix} V_{md} \\ V_{mq} \\ 0 \end{pmatrix} \quad (10)$$

Using equation (10), the reference input to the PWM modulator is derived as follows:

$$V_{sd} = V_{md} + L\omega I_{sq} - \left(RI_{sd} + L\frac{dI_{sd}}{dt}\right) \quad (11)$$

$$V_{sq} = V_{mq} - L\omega I_{sd} - \left(RI_{sq} + L\frac{dI_{sq}}{dt}\right) \quad (12)$$

Equations (11) and (12) are realized to establish the 24-pulse converter operation in the closed loop control scheme.

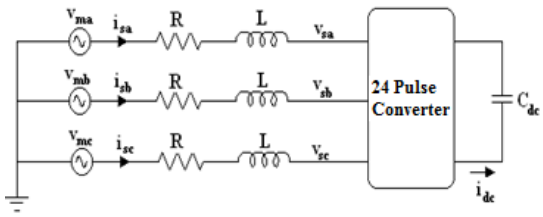

Fig .16. Equivalent circuit of AC-to-DC conversion.

B. Control Strategy

A complete closed loop control scheme for operating the 24-pulse rectifier with the unity power factor on the input side is shown in Fig.18. The objective of the control loop is to maintain the DC voltage at the desired reference value and to control the active power flow from AC grid to the DC side. A set of capacitors are used at the DC bus to support the dc link voltage at the desired value to make the real power balance between the two sides of the converter. This is the most important for a successful operation of the HVDC system. It requires two control loops namely the outer voltage control loop and the inner current control loop. The outer DC voltage controller sets the real current reference for the inner current controller. The reactive current reference is set to zero for achieving the unity power factor. In the inner current controller, a decoupled current control strategy is employed in order to independently control the real and the reactive power components.

A phase-locked loop is used to determine the instantaneous angle θ of the three-phase line voltage. The three-phase voltages and the supply currents are transformed into two-phase quantities using Park's transformation, which gives d – q axis voltage and current for the controller. The d-axis reference current i_{sd}^* obtained from the DC voltage controller is compared

with the actual d axis current and is stabilized through the PI controller to get the equivalent d axis reference voltage. Similarly, the actual q axis current i_q is compared with the reference current i_{sq}^* which is set to zero for achieving the unity power factor, and the error so obtained is stabilized through another PI controller to get the equivalent q axis reference voltage. The parameters of these PI controllers are tuned, and their values are tabulated in Table 3. Further more, the equations (11) and (12) are realized in the inner current control loop in order to obtain the reference wave for the PWM modulator.

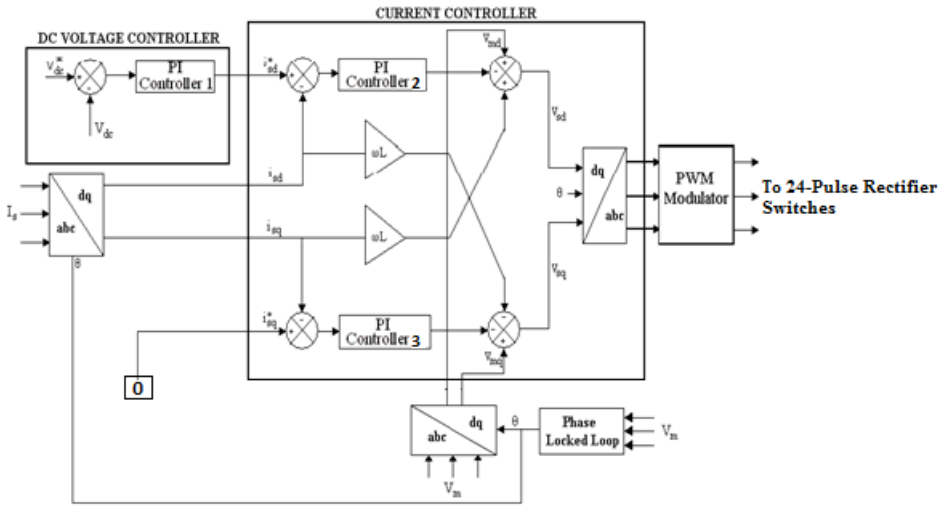

Fig .17. Closed loop control scheme.

Table 3. PI controller parameters.

PI controller	K_P	K_I
PI_1	0.5	2.5
PI_2	1.8	6
PI_3	7	4.3

7. Simulation results and discussion

In this section, the behaviour of the VSC-based HVDC transmission system will be analyzed using MATLAB/Simulink. Thus, in order to test the closed loop control scheme and to test the behaviour of the system, suitable case studies are carried out under steady state and dynamic operation.

A. Steady State Condition

A constant power is made to flow from one station to the other, and the behaviour of the system is demonstrated in Fig 19. The reference real power command is set at 100MW and reactive power is maintained at zero throughout the steady-state operation. In Fig 19.a, Station 1 voltage and current, real power (P) supplied to the system, reactive power (Q), DC link voltage V_{dc}, and the current through the DC link are shown to demonstrate the behaviour of the rectifier during the steady state operation of the VSC based HVDC systems. The relation between the phase voltage and phase current is separately highlighted in Fig 19.b to show that they are in phase with each other

resulting to the unity power factor operation. In Fig 19.c, Station 2 voltage and current, real power (P) absorbed from the system, reactive power (Q), DC link voltage V_{dc} and the current I_{dc} are shown to demonstrate the steady state behaviour of the inverter station during the same operation.

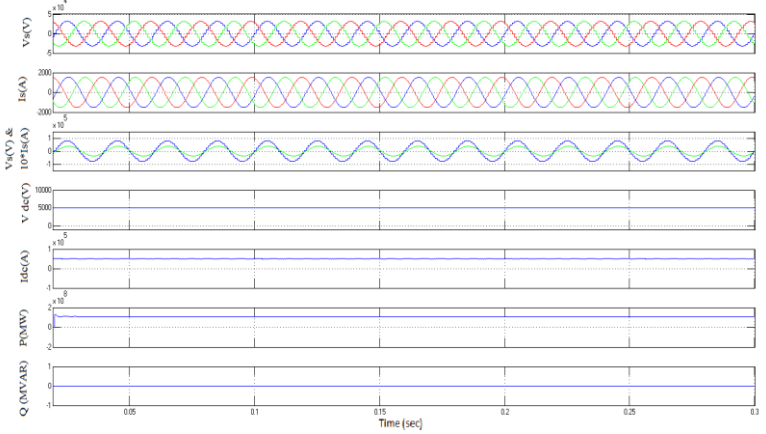

Fig .19. (a) Waveforms at the rectifier station during the steady state condition.

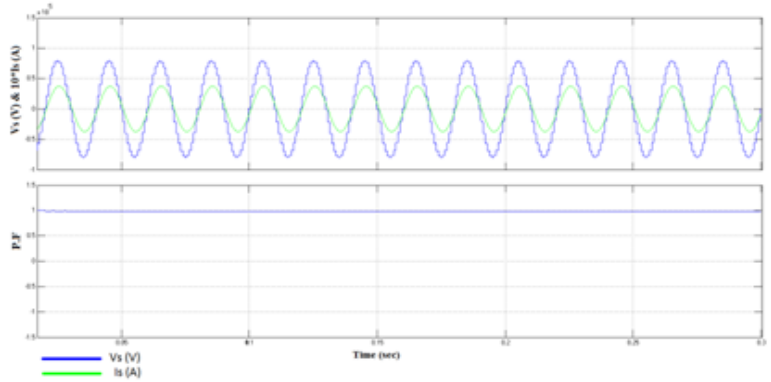

Fig .19. (b) Waveforms of phase voltage and current at the steady state condition.

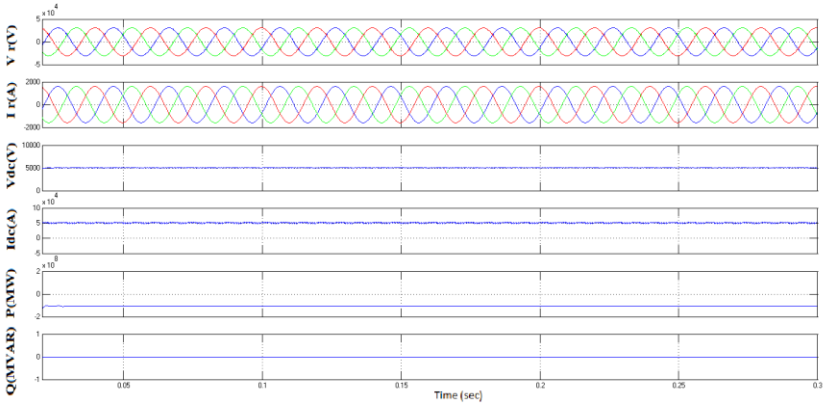

Fig.19. (c) Waveforms at the inverter station during the steady state condition.

B. Dynamic Condition

Fig. 20 shows the dynamic behaviour of the 24-pulse voltage source converters. The reference real power command is initially set at 50 MW. Later at t = 0.2s, the real power reference is suddenly increased to 100 MW, and it is maintained at this value. In Fig 20.a, the converter station 1 parameters are shown to demonstrate the behaviour of the rectifier during the dynamic operation of VSC based HVDC systems. This fig depicts that irrespective of load variation the DC link voltage is maintained at its set reference value of 5000 V and that the reactive power is maintained at 0 so as to achieve the unity power factor operation. Fig 20.b, depicts the voltages and currents related to the converter station 2. Fig 20.c shows that the phase voltage and phase current are in phase with each other as the reactive power is maintained at zero irrespective of the variation of load, and hence the power factor is unity.

C. Converter stations operating at two different frequencies

Converter station 1 operates at 50Hz frequency and station 2 at 60 Hz frequency. Hence in the simulation parameters discussed in Table 3, the value of the inductor L2 is changed to 5.7mH. Also the transformer frequency is changed. The reference real power command is initially set at 50 MW. Later at t = 0.2s, the real power reference is suddenly increased to 100 MW, and this value is maintained thereafter. In Fig 21.a, various parameters related to station 1, whose operating frequency is 50 Hz, are depicted. In Fig 21.b, shows the converter station 2 voltages and currents which are operated at 60 Hz frequency. Fig 21.c shows the unity power factor operation by highlighting the phase relation between the voltage and the current. Furthermore, Fig 21.d separately highlights the differences in the operating frequency of the converter stations 1 and 2, respectively.

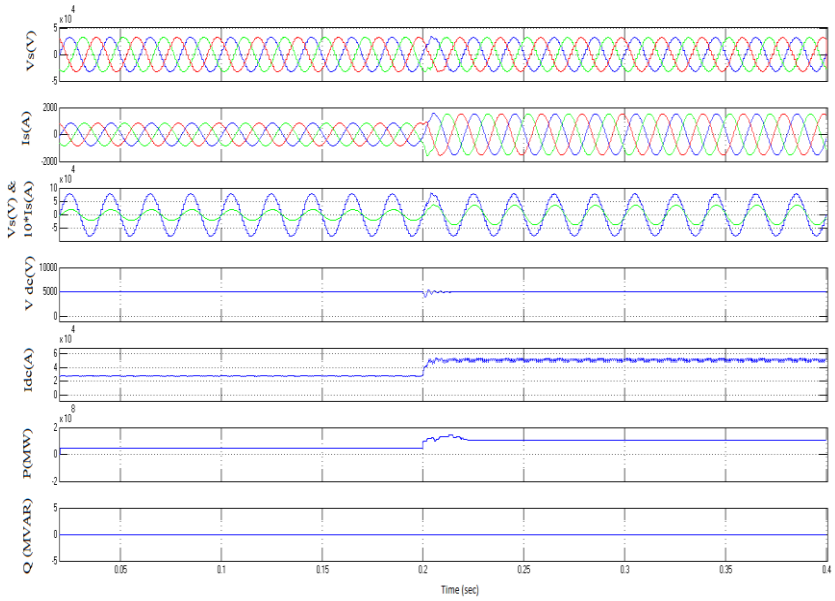

Fig. 20. **(a)** Waveforms at the rectifier station during the dynamic power change.

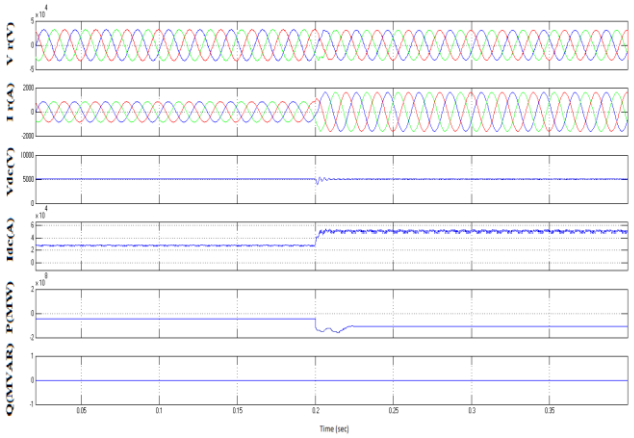

Fig .20. **(b)**Waveforms at the inverter station during the dynamic power change.

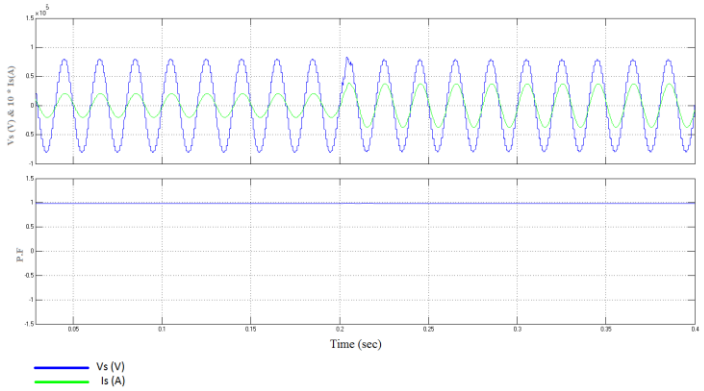

Fig. 20. **(c)**Waveforms of phase voltage and current during the dynamic condition.

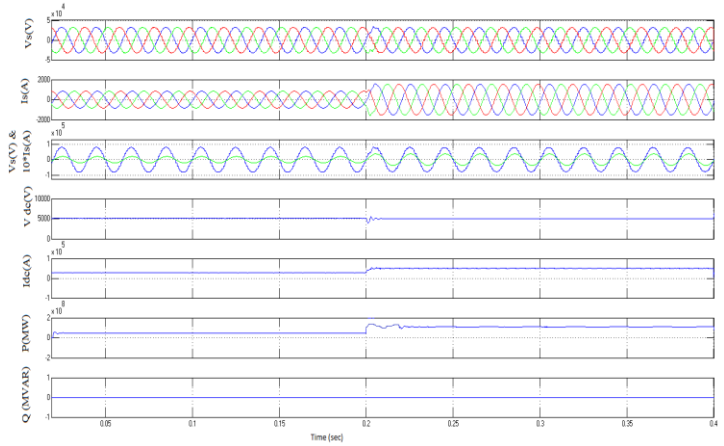

Fig .21. **(a)** Waveforms at the station 1 for systems operating with two different frequencies.

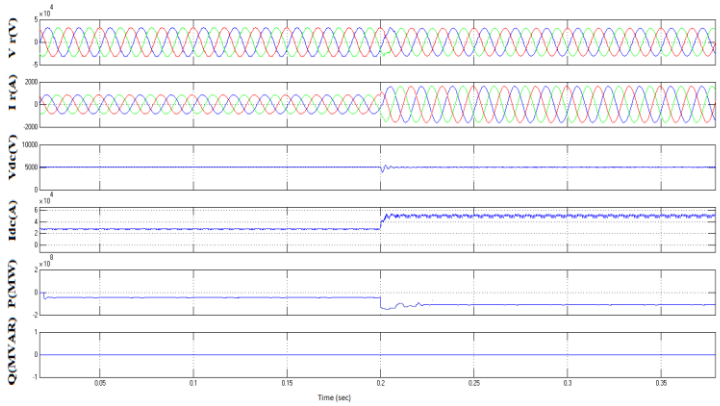

Fig. 21. (b) Waveforms at the station 2 for systems operating with two different frequencies.

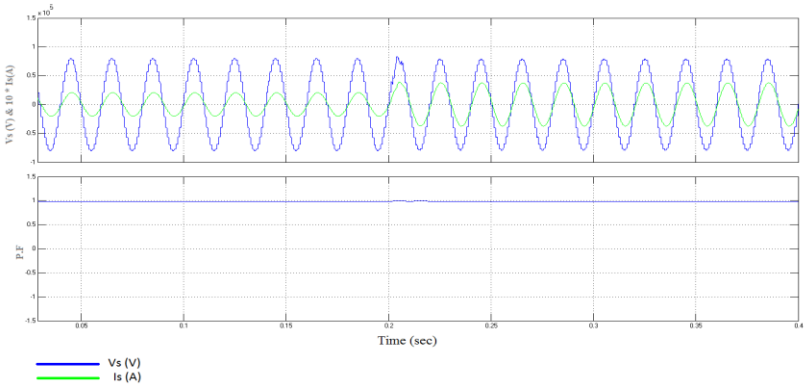

Fig. 21. (c) Waveforms of phase voltage and current for systems with different frequencies.

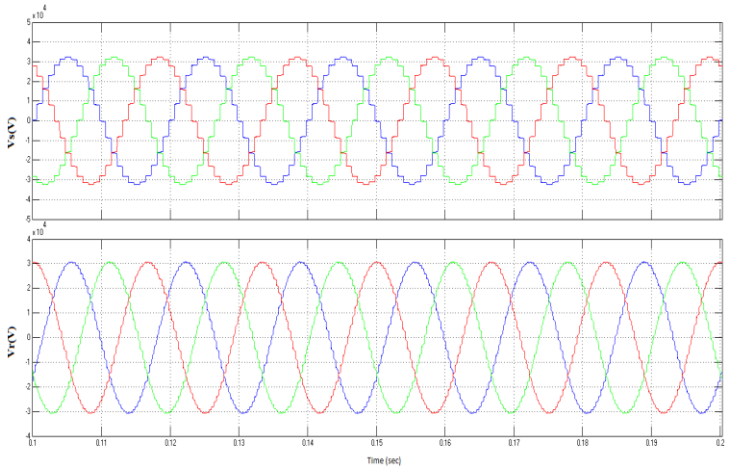

Fig .21. (d) Converter station 1 and 2 voltages at different frequencies.

8. Conclusion

The application of power electronics started with the emergence of high voltage direct current system. Although HVDC was a feasible solution for efficient long distance bulk power transmission, accompanying harmonic currents had been a great challenge. Hence in the present work, the design of a rectifier and in inverter for a significant reduction of harmonics has been done. For the elimination of harmonics of supply current, a 24-pulse rectifier based on a star-connected transformer has been designed. The analysis of the proposed inverter obtained by combining the multipulse-multilevel inverter topologies shows that there is a drastic reduction in total harmonic distortion. A proper selection of the dead angle for a multi level inverter, in the combined topology would yield better harmonic performance. The closed loop controller based on decoupled control strategy has been developed and found to be effective over a wide range of power system operating conditions. The behaviour of the proposed 24-pulse VSC based HVDC system has been analyzed under steady state dynamic operating conditions for stations with a single frequency and stations with different frequencies. The steady state and dynamic performances describes the ability of a control algorithm for a successful operation of the proposed converter in a HVDC system.

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