CMOS High Frequency/Low Voltage Full-Wave Rectifier

Adisak Monpapassorn
Department of Electronic Engineering, South-East Asia University,
Bangkok 10160, Thailand

Abstract

A CMOS high frequency/low voltage full-wave rectifier is presented. The proposed rectifier is composed of three main components: a dual output V-I converter, a positive full-wave current rectifier, and an I-V converter. A voltage input signal is changed into two out-of-phase current signals by the V-I converter. The current rectifier rectifies these current signals resulting in a positive full-wave current output signal that is finally changed into a positive full-wave voltage output signal by the I-V converter. The theory of operation is described, and the simulation results obtained from the PSPICE program are used to verify the theoretical prediction. Simulation rectifier performance with a 0.5 μm MOS model obtained through MIETEC, using a ± 1.2 V supply voltage, demonstrates good rectifier integrity at operation frequencies up to 100 MHz.

Keywords: CMOS, full-wave rectifier, dual output V-I converter, I-V converter.

1. Introduction

Rectifiers are extensively used in wattmeters, AC voltmeters, RF demodulators, piecewise linear function generators, and various nonlinear analog signal-processing circuits. The operations of diode rectifiers are limited by the threshold voltages of diodes, approximately 0.3 V for germanium diodes and 0.7 V for silicon diodes, thus diode rectifiers are used only in some applications in which the precision in the range of threshold voltage is insignificant, such as radio frequency demodulators and DC voltage supply rectifiers. Nevertheless, for the applications requiring high accuracy, diode rectifiers cannot be used. This can be overcome by using integrated circuit rectifiers instead.

One classical problem with integrated circuit rectifiers based on diodes and opamps is that during the non-conduction/conduction transition of the diodes, the opamps must recover with a finite small-signal dV / dt resulting in significant distortion during the zero-crossing of the input signal. The use of the high slew-rate opamps does not solve this fundamental drawback because it is a small-signal transient problem [1]. Conventional rectifiers are thus limited to a frequency performance well below the gain-bandwidth product or f_T of the amplifier [2]. This limitation is improved by designing rectifiers with current mode techniques [1-7]. Some of these current mode rectifiers use the CMOS class AB amplifiers to separate the positive and negative currents [3-4]. Although there are a few partial devices, they also have a drawback that while $-4I_B < I_{in} < 4I_B$, where I_{in} is an input current and I_B are two constant current sources used in the CMOS class AB amplifier; the output current has square and offset errors, which are the errors of the low-level signal. The use of current mode rectifiers employing current conveyors and diodes can avoid these errors. Recently, rectifiers employing current conveyors and diodes have received wide attention. For example, LTP Electronics Ltd. [5] and Khan *et al.* [7] proposed the same current conveyor full-wave rectifiers as shown in Fig. 1(*a*). This full-wave rectifier is developed to reduce the distortion due to the small-signal dV / dt limitation by Toumazou *et al.* [2] with the addition of a DC voltage source as shown in Fig. 1(*b*). Hayatleh *et al.* [6] further developed this full-wave rectifier to reduce the effect of temperature on the zero-crossing performance using a current source and a resistor in place of the voltage source as shown in Fig. 1(*c*).

In this paper, the author presents a CMOS high frequency/low voltage full-wave rectifier using a similar idea to the above current conveyor rectifiers. Namely, it uses a V-I

converter to change an input voltage into currents, diodes to rectify these currents resulting in a positive full-wave current, and an I-V converter to change the positive full-wave current into a positive full-wave voltage. However, the proposed rectifier has features superior to the above current conveyor rectifiers, as follows:

i) Each of the above current conveyor rectifiers uses a passive resistor and two current conveyors as devices in its V-I converter while the proposed rectifier uses a dual output all MOS V-I converter that is specially designed. Hence the proposed rectifier uses fewer devices. Further, the proposed rectifier is more suitable for IC fabrication than the above current conveyor rectifiers. (i.e. it needs no passive resistor).

ii) Each of the above current conveyor rectifiers employs high power consumption and supply voltage (needed by current conveyors), and has a low operating frequency (dependent on the operating frequencies of current conveyors). With the advantage of the specially designed V-I converter, the proposed rectifier employs power consumption of approximately 1 mW and uses a ± 1.2 V supply voltage. Furthermore, it provides an operation frequency up to 100 MHz (simulation result with 0.5 μm MOS model obtained through MIETEC)

iii) Some current conveyor rectifiers [5,7] do not use a diode bias voltage (i.e. it is 0 V) thus they have the problem of the non-conduction/conduction transition of diodes at high frequency. Some current conveyor rectifiers [2,6] use a stable voltage to bias diodes in the rectifier in order to make the diodes turn-on all the time to solve the problem of the non-conduction/conduction transition. This voltage is equal to approximately $2V_H$, where V_H is the threshold voltage of the diodes. V_H depends upon the temperature [6]: when the temperature increases, it causes an offset voltage at the output; inversely, when the temperature decreases, it causes diodes not to turn-on all the time. The proposed rectifier uses the diode bias voltage $2V_H$ at the series two diodes. This voltage depends on the temperature of the diodes, the same as the voltage $2V_H$ of the series two diodes in the rectifier. Thus the proposed rectifier has much better temperature stability than either of the current conveyor rectifiers.

2. Proposed full-wave rectifier

The proposed rectifier is shown in Fig. 2(*a*). It consists of three main components: a V-I converter, a current rectifier, and an I-V converter. The V-I converter is composed of MI1 to MI5, M1 to M14, MA, MB, and I_{B1}. The operation of the V-I converter is as follows: Using MI1 to MI5 with the same characteristics, I_{B1} is mirrored by MI1, MI2, MI4, and MI5 to the drain of M1 and it is also mirrored by MI1 and MI3 to the drain of M3; hence, the drain currents of M1 (I_{D1}) and M3 (I_{D3}) are equal. Using closely matched M1 to M4, the input voltage is thus followed to node A, voltage buffer action, [8,9]. This voltage makes the current I_1 flowing through a MOS-resister R_1 (MA and MB) [10]. I_1 can be expressed as

$$I_1 = V_{in}(2KV_{DT}) \tag{1}$$

where MA and MB have the same characteristics; $K = \mu C_{ox}W/L$, μ is the mobility of carriers, C_{ox} is the gate capacitance per unit area, W and L are the channel width and length; $V_{DT} = V_{DD}-V_T = -(V_{SS}+V_T)$, $V_{DD} = -V_{SS}$, V_T is the threshold voltage.

In fact, the output resistance (r_{out}) of the buffer has to be much higher than R_1, to obtain $V_A = V_{in}$. The output resistance of the buffer is

$$r_{out} = (g_{m2} + g_{m4})^{-1} \tag{2}$$

where g_{mn} is the transconductance of Mn. For MOS operating in saturation mode [11], the transconductance is given by

$$g_m = \sqrt{2\mu C_{OX}(W/L)I_D} \tag{3}$$

Due to $V_{in} = V_A$, M1 and M2 as well as M3 and M4 are the current mirrors, resulting in $I_{B1} = I_{D1} = I_{D2} = I_{D3} = I_{D4}$. Using (2) and (3), one finds that r_{out} depends on I_{B1} and the W/L of M1 to

M4. Namely, if I_{B1} and W/L are high, r_{out} will be low.

I_1 is mirrored by M5, M6, M10, and M11 through node B as I_1 and it is also mirrored by M5, M7, M8, M9, M10, M12, M13, and M14 through node C as $-I_1$. The out-of-phase currents, I_1 and $-I_1$, are fed into the current rectifier. The current rectifier is composed of MOS-diodes: MD1, MD2, MD3, MD4, MD5, MD6; the constant current source I_{B2}; and the buffer A_1. Although the diode can be created in the CMOS process, it will be easier in fabrication if the circuit consists of one kind of device. Thus, the author uses MOS-diodes in place of diodes. The operation of the current rectifier is as follows: MD1, MD2, MD3, MD4, MD5, and MD6 operate as diodes, (see Fig. 2(*b*)). MD5, MD6, and I_{B2} are joined to create the bias voltage supply to the anodes of MD2 and MD3 through A_1. The circuit of A_1 is shown in Fig. 2(*c*). Its operation is the same as the buffer (I_{B1}, MI1-MI5, and M1-M4) explained above. A_1 is used to protect the effects of the load, the I-V converter, and the outputs of V-I converter on the voltage at the anode of MD5. The bias voltage must be the minimum voltage that can make MD2 and MD1 as well as MD3 and MD4 turn-on all the time, to get the minimum offset voltage at the output, which is carried out by adjusting I_{B2}. From the operation of the V-I converter, when I_1 is positive, $-I_1$ is negative, MD1 and MD3 are turned on, MD2 and MD4 are turned off; hence, I_1 is the output current, I_2. In the opposite way, when I_1 is negative, $-I_1$ is positive, MD1 and MD3 are turned off, MD2 and MD4 are turned on; therefore, $-I_1$ is I_2. Using (1), the relation between V_{in} and I_2 can be written as

$$\left.\begin{aligned} V_{in} > 0;\ \ I_2 &= V_{in}(2KV_{DT}) \\ V_{in} < 0;\ \ I_2 &= -V_{in}(2KV_{DT}) \end{aligned}\right\} \qquad (4)$$

R_2 consists of MC and MD operating as an I-V converter that converts I_2 to the output voltage. Using $R_2 = R_1$, the output voltage can be obtained as

$$\left.\begin{aligned} V_{in} > 0;\ \ V_{out} &= V_{in} \\ V_{in} < 0;\ \ V_{out} &= -V_{in} \end{aligned}\right\} \qquad (5)$$

This means that the proposed circuit operates as a positive full-wave voltage rectifier.

The supply voltage must be enough to make M2 and M4 operate in the saturation mode the same as M1 and M3; hence, we can express the minimum supply voltage as

$$\left.\begin{aligned} V_{SS(\min)} &= -\left(|V_{eff4}| - |V_{eff10}| - |V_{TP}| - |V_{TN}|\right) \\ V_{DD(\min)} &= |V_{eff2}| + |V_{eff5}| + |V_{TN}| + |V_{TP}| \end{aligned}\right\} \qquad (6)$$

where $V_{eff} = V_{GS} - V_T = \sqrt{\dfrac{2I_D}{\mu C_{OX}(W/L)}}$ [11]

This leads to the minimum and maximum input voltage as

$$\left.\begin{aligned} V_{in(\min)} &= V_{SS} + |V_{eff4}| + |V_{eff10}| + |V_{TP}| + |V_{TN}| \\ V_{in(\max)} &= V_{DD} - |V_{eff2}| - |V_{eff5}| - |V_{TN}| - |V_{TP}| \end{aligned}\right\} \qquad (7)$$

The linear operation range is

$$operation\ range = V_{in(\max)} - V_{in(\min)} \qquad (8)$$

3. Simulation results

To verify the theoretical design, the proposed rectifier was simulated by using the PSPICE program with a 0.5 μm MOS model obtained through MIETEC as listed in Table 1. Both W/L parameters of MOSs and constant current sources of the proposed rectifier in Fig. 2 are listed in Table 2. The supply voltages used are ± 1.2 V. The DC transfer characteristic of the proposed rectifier is shown in Fig. 3, which displays the operation range from -300 mV to 300 mV of the input voltage, equations (7) and (8). In this operation range, the simulation power consumption is roughly 1 mW. The magnified zero-crossing of Fig. 3 is shown in Fig. 4 in which the blunting region is found as $-5\ \text{mV} \le V_{in} \le 5\ \text{mV}$. Applying sine waves (100 mV_{peak}) having the frequencies of 1 MHz, 10 MHz, and 100 MHz; $I_{B2} = 0.1$ μA; the input and output signals at each frequency are shown in Fig. 5, Fig. 6, and Fig. 7, respectively. At the frequency of 100 MHz, simulated without the bias voltage, $I_{B2} = 0$ μA, one obtains the input and output signals as shown in Fig. 8. It is

evident in Fig. 8 that each initial rise-time of the full-wave signal has an error due to the on-off transition problem of diodes in the current rectifier. It is clearly seen in Fig. 7 and Fig. 8 that, using the bias voltage to solve the on-off transition problem of diodes, the proposed rectifier yields the operation frequency up to 100 MHz. However, this operation frequency is obtained only from simulation. When the proposed rectifier is built as an IC, the operation frequency will be lessened by the effect of parasitic capacitance in the IC. Fig. 9 shows the output voltage versus the frequency. The output voltage is initially decreased at the frequency of 1.62 MHz and it is decreased to a –3 dB cutoff point at the frequency of 34.33 MHz. Fig. 10 shows the temperature stability of the proposed rectifier at zero-crossing, which is simulated at the temperatures: 25°C, 50°C, and 70°C by applying a sine wave input (100 mV_{peak}, 1 MHz). The shifts in voltages of signals in Fig. 10 between the temperatures of 25°C and 50°C, and 50°C and 70°C are 136 μV and 164.9 μV, respectively. These indicate good temperature stability of the proposed rectifier.

4. Conclusions

In this paper, the author has reported the design of a CMOS high frequency/low voltage full-wave rectifier. The proposed rectifier is based on the previously reported current conveyer rectifiers. However, with a different circuit structure, the proposed rectifier yields better features over the previously reported current conveyor rectifiers, in view of the employed voltage, the power consumption, the number of devices, the operation frequency, the stability of temperature, and the simplicity for IC fabrication. The proposed rectifier uses a ±1.2 V supply voltage and has an operation voltage range from –300 mV to 300 mV. In addition, it has an operation frequency up to 100 MHz; however, this operation frequency is obtained only from simulation. When the proposed rectifier is built as an IC, the operation frequency will be lessened by the effect of parasitic capacitance in the IC. The proposed rectifier is suitable for a building block in low voltage/high frequency analog signal processing circuits.

5. References

[1] Lidgey, F. J., Hayatleh, K., and Toumazou, C., New Current-Mode Precision Rectifiers, Proc. IEEE Int. Symp. on Circuits and Syst., Chicago, pp. 1322-1325, 1993.

[2] Toumazou, C., Lidgey, F. J., and Chattong, S., High Frequency Current Conveyor Precision Full-Wave Rectifier, Electron. Lett., Vol. 30, pp. 745-746, 1994.

[3] Ramirez-Angulo, J., High Frequency Low Voltage CMOS Diode, Electron. Lett., Vol. 28, pp. 298-300, 1992.

[4] Surakampontorn, W., and Riewruja, V., Integrable CMOS Sinusoidal Frequency Doubler and Full-Wave Rectifier, Int. J. Electron., Vol. 73, pp. 627-632, 1992.

[5] LTP Electronics Ltd., CCII01 Current-Conveyor Data Sheet, Oxford, 1993.

[6] Hayatleh, K., Porta, S., and Lidgey, F. J., Temperature Independent Current Conveyor Precision Rectifier, Electron. Lett., Vol. 30, pp. 2091-2093, 1994.

[7] Khan, A. A., Abou el-ela, M., and Al-Turaigi, M. A., Current-Mode Precision Rectification, Int. J. Electron., Vol. 79, pp. 853-859, 1995.

[8] Battersby, N., and Toumazou, C., Class AB Switched-Current Memory for Analogue Sampled-Data System, Electron. Lett., Vol. 27, pp. 873-875, 1991.

[9] Bruun, E., A Dual Current Feedback CMOS Op Amp, Proc. 10th NORCHIP Seminar, Helsinki, Finland, 1992.

[10] Wang, Z., 2-MOSFET Transresistor with Extremely Low Distortion for Output Reaching Supply Voltages, Electron. Lett., Vol. 26, pp. 951-952, 1990.

[11] Johns, D., and Martin, K., Analog Integrated Circuit Design, John Wiley & Sons, 1997.

```
.MODEL NM NMOS LEVEL=3
+UO=460.5 TOX=1.0E-8 TPG=1 VTO=0.62 JS=1.08E-6
+XJ=0.15U RS=417 RSH=2.73 LD=0.04U VMAX=130E3
+NSUB=1.71E17 PB=0.761 ETA=0.00 THETA=0.129 PHI=0.905
+GAMMA=0.69 KAPPA=0.10 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10
+MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10
+KF=3.07E-28 AF=1 WD=+0.11U DELTA=+0.42 NFS=1.2E11
+DELL=0U LIS=2 ISTMP=10 TT=0.1E-9

.MODEL PM PMOS LEVEL=3
+UO=100 TOX=1.0E-8 TPG=1 VTO=-0.58 JS=0.38E-6
+XJ=0.10U RS=886 RSH=1.81 LD=0.03U VMAX=113E3
+NSUB=2.08E17 PB=0.911 ETA=0.00 THETA=0.120 PHI=0.905
+GAMMA=0.76 KAPPA=2 CJ=85E-5 MJ=0.429 CJSW=4.67E-10
+MJSW=0.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10
+KF=1.08E-29 AF=1 WD=+0.14U DELTA=0.81 NFS=0.52E11
+DELL=0U LIS=2 ISTMP=10 TT=0.1E-9
```

Table 1 MOS model that is used in simulation.

M1-M5, M8-M10, M13-M14, MI1-MI5, MI6-MI10	20 μm / 0.6 μm
M6, M11	26.5 μm / 0.6 μm
M7, M12	26.9 μm / 0.6 μm
M15-M18	100 μm / 0.6 μm
MA-MD	2 μm / 2 μm
MD1-MD6	2 μm / 0.6 μm
I_{B1}	20 μA
I_{B2}	0.1 μA
I_{B3}	100 μA

Table 2 W / L parameters and constant current sources of the circuit in Fig. 2.

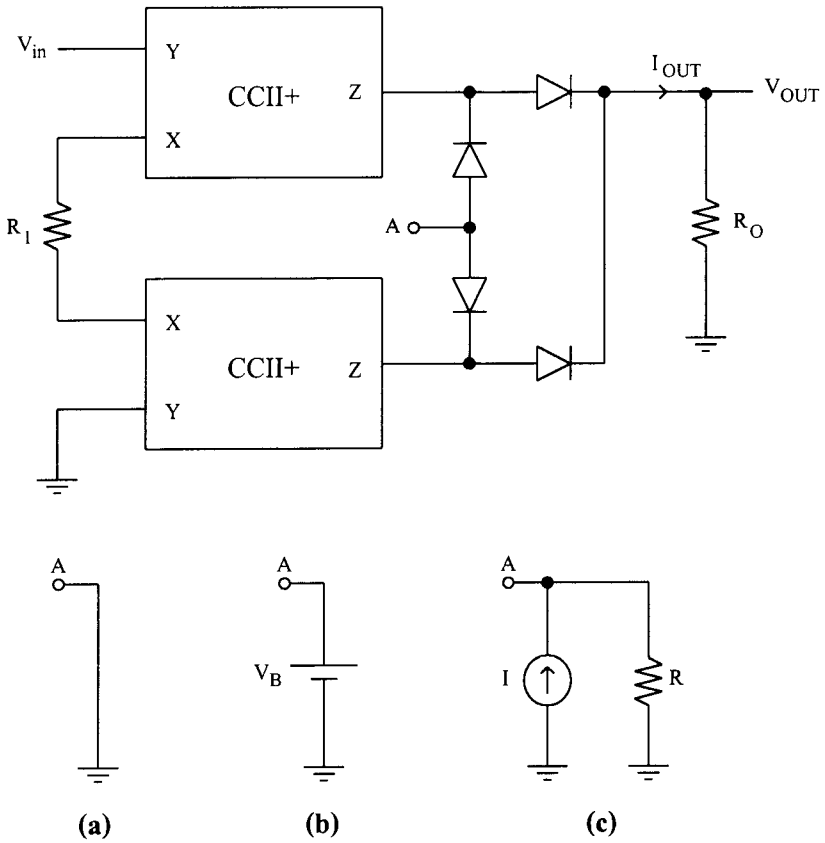

Figure 1. Current conveyor based precision full-wave rectifiers: (a) proposed by LTP Electronics Ltd. [5] and Khan et al. [7], (b) voltage biasing technique proposed by Toumazou et al. [2], and (c) current biasing technique proposed by Hayatleh et al. [6].

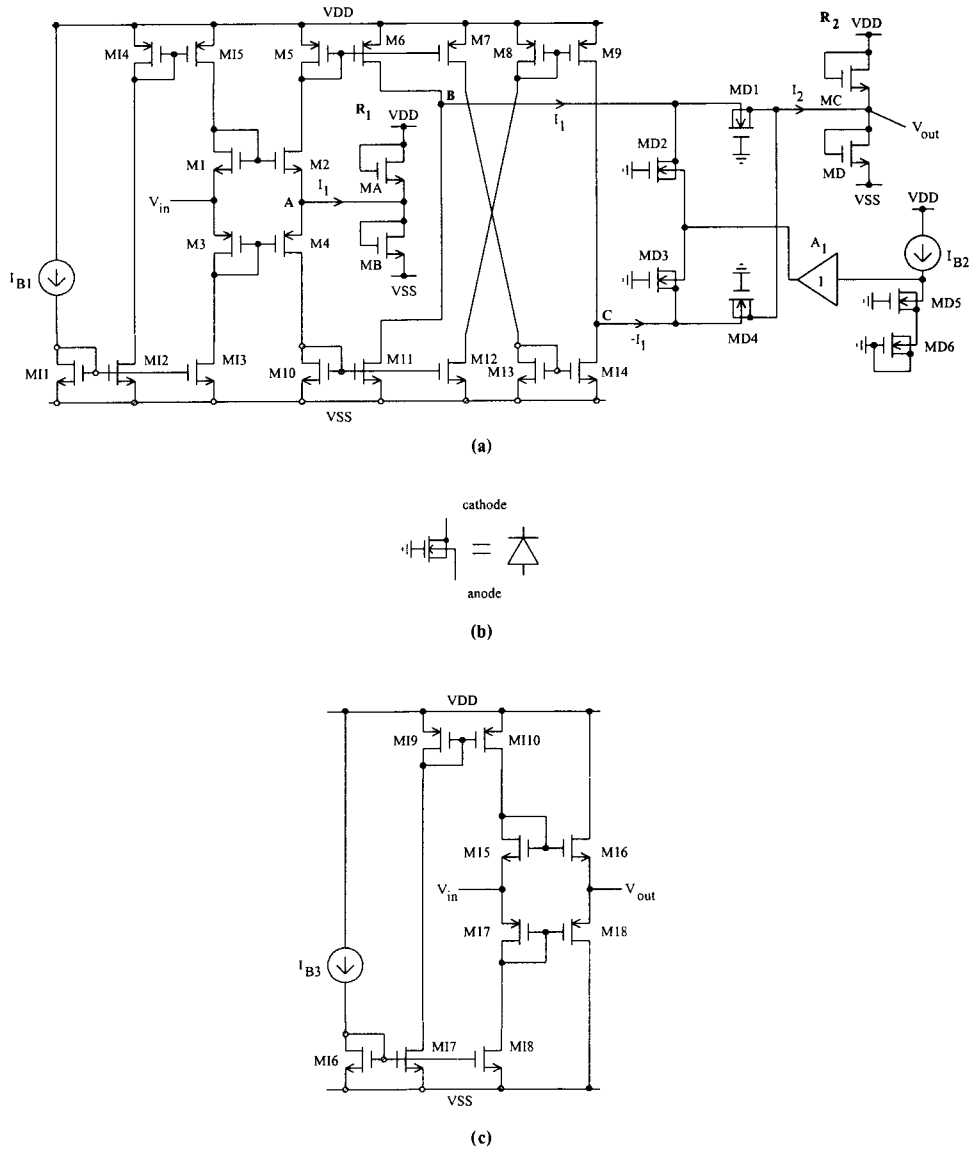

Figure 2. Proposed high frequency/low voltage full-wave rectifier: (a) rectifier, (b) substituting a diode with MOS, and (c) A_1 voltage buffer circuit.

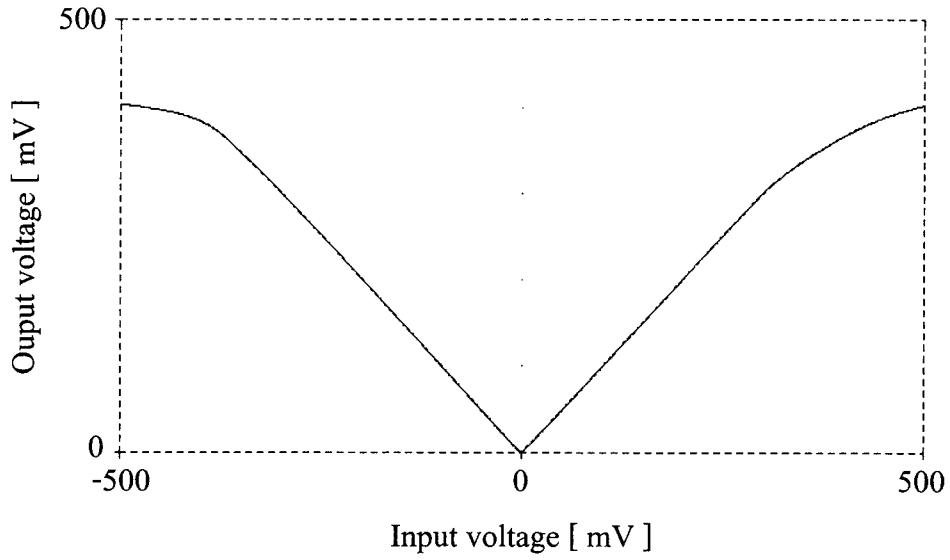

Figure 3. DC transfer characteristic of the proposed rectifier.

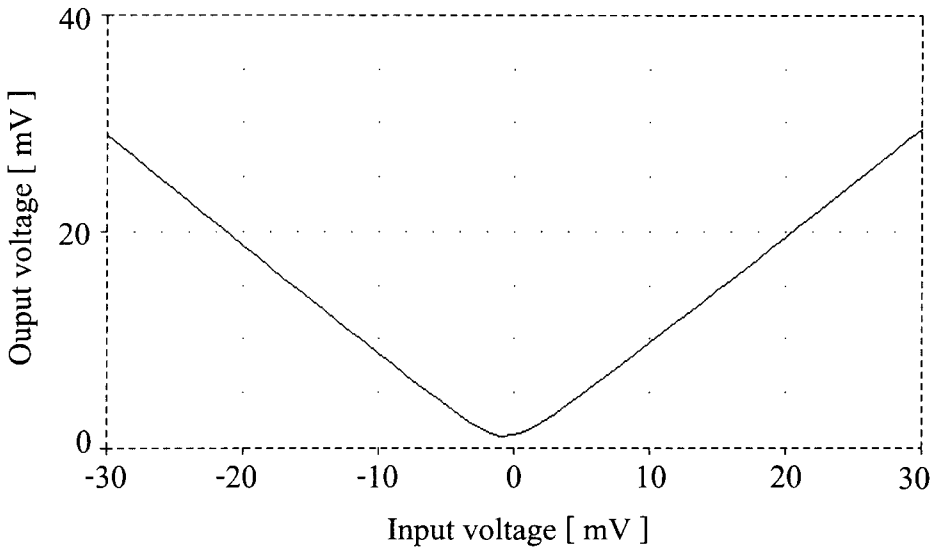

Figure 4. Magnified zero-crossing of Fig. 3.

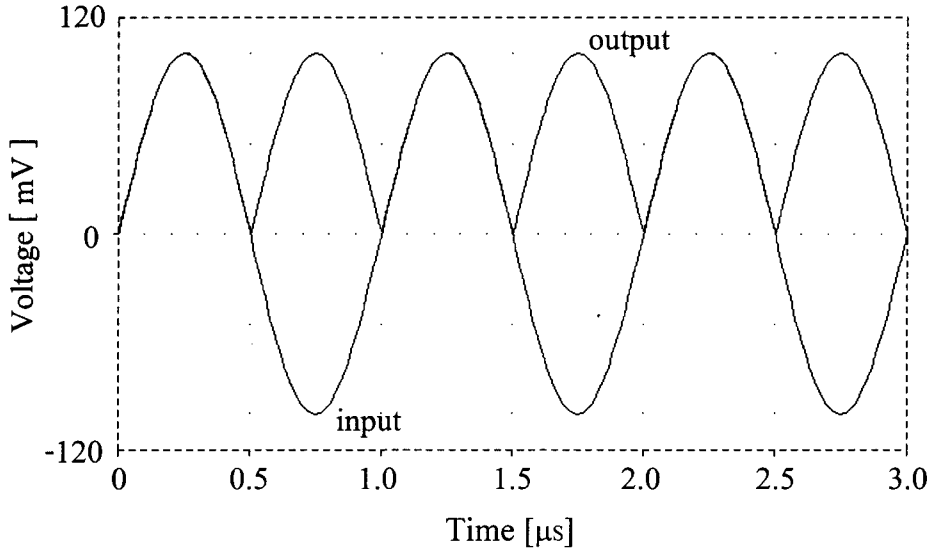

Figure 5. Input and output of the proposed rectifier at the frequency of 1 MHz with the bias voltage.

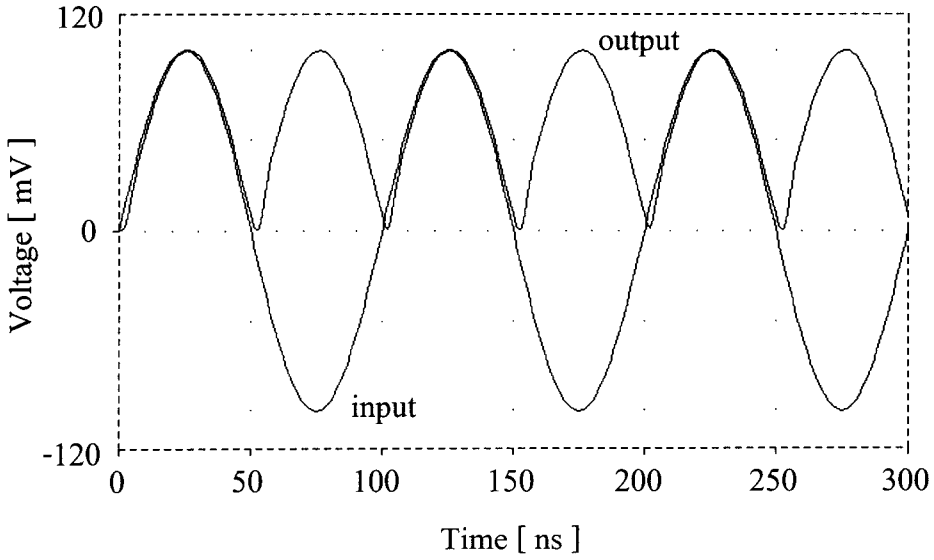

Figure 6. Input and output of the proposed rectifier at the frequency of 10 MHz with the bias voltage.

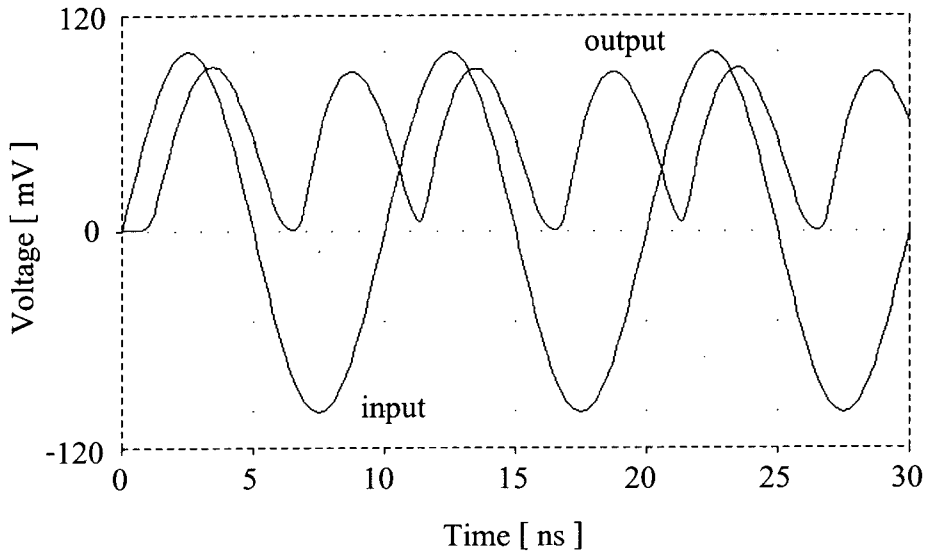

Figure 7. Input and output of the proposed rectifier at the frequency of 100 MHz with the bias voltage.

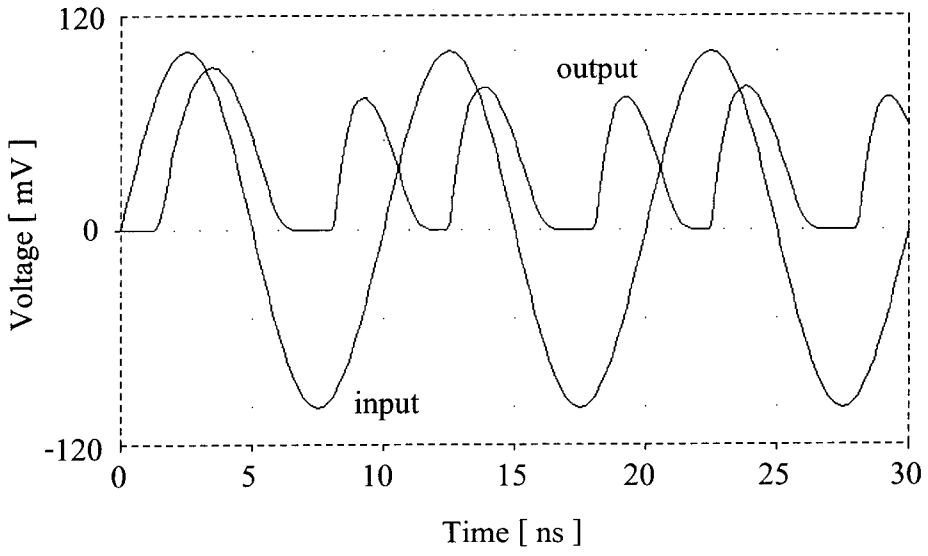

Figure 8. Input and output of the proposed rectifier at the frequency of 100 MHz without the bias voltage.

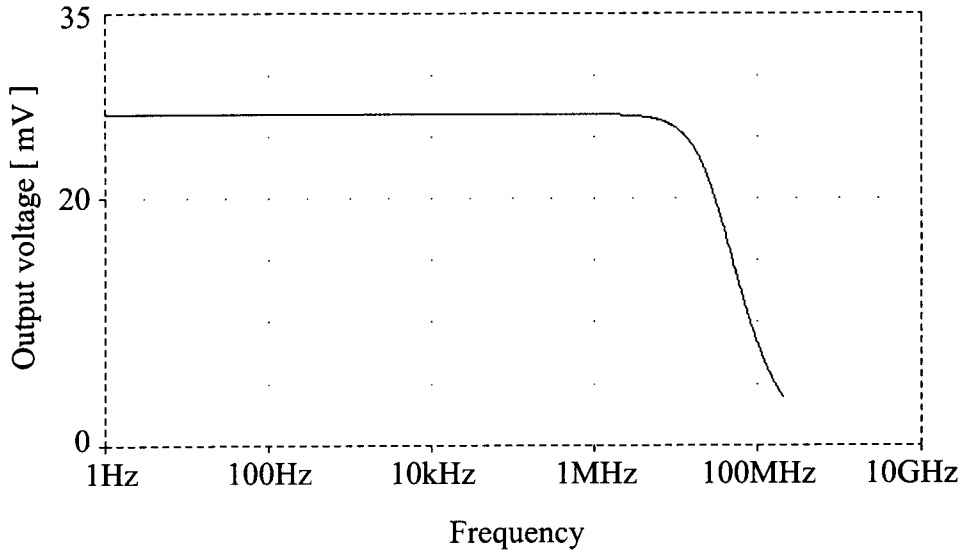

Figure 9. Output voltage of the proposed rectifier versus the frequency.

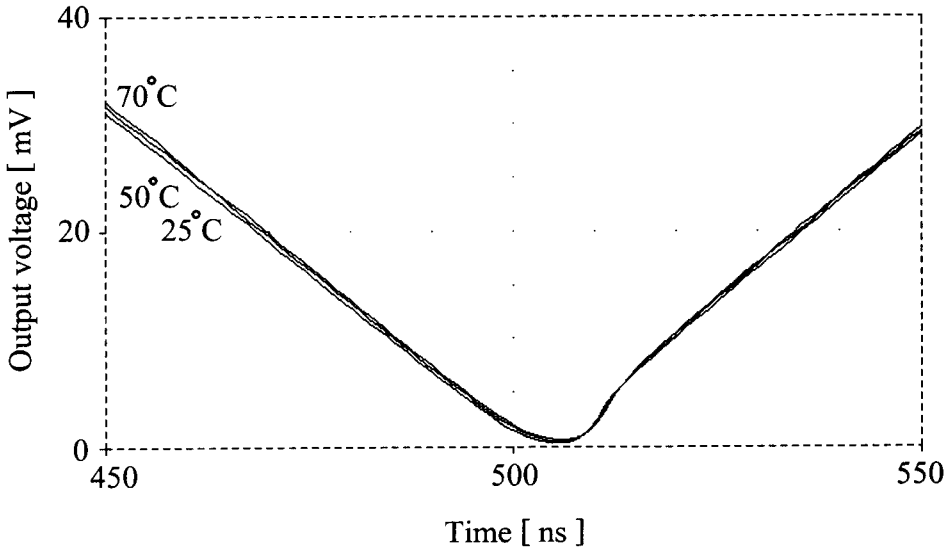

Figure 10. Zero-crossing of the proposed rectifier for some temperatures.