High Frequency/Low Voltage CMOS Adder

Adisak Monpapassorn
Department of Electronic Engineering, South-East Asia University, Bangkok 10160, Thailand

Abstract

A high frequency/low voltage CMOS adder is presented. Two main components in the proposed adder are i) the V to I circuit which uses two MOSs and two constant current sources and ii) the I to V circuit which uses two MOSs. The proposed adder uses two V to I circuits and one I to V circuit for the first adder function. The next adder functions can be obtained by increasing one V to I circuit per one next adder function. The theory of operation is described and simulated results obtained from PSPICE program are used to verify the theoretical prediction. Simulated adder performance with 0.8 μ m MOS technology shows that the output operating voltage range given an error voltage less than 1 % is 775 mV when using the power supplies of ± 1.5 VDC and a frequency response up to 125 MHz.

1. Introduction

Analog CMOS signal processing circuits have received significant attention. One of them is an analog adder that is used as an important building block in analog computation [1-2] and in fuzzy control [3]. A well-known adder is an opamp adder. One advantage of the opamp adder is, it has a wide operating voltage range. However it also has disadvantages, using many transistors and using passive devices, which are the cause of the use of the large chip area. One way to avoid these drawbacks is the use of CMOS adders [4-6]. The operations of these adders are performed in current mode since the currents can be directly summed using Kirchhoff's law. This paper proposes a CMOS voltage adder operating in current mode, the same as CMOS adders [4-6], namely it uses the V to Is to convert input voltages into input currents and the I to V to convert the sum of input currents into the output voltage. Nevertheless the proposed adder uses the supply voltages lower than [4-5]. Additionally, owing to the proposed adder using 0.8 μm MOS technology, it has an operating frequency higher than [4-6].

2. Circuit Description

The proposed V to I circuit is shown in Fig.1a. All MOSs are biased in saturation region. The source current of M_P can be expressed as

$$I_{S(M_P)} = \beta_P \left(V_{DD} - |V_{TP}| - V_{in}\right)^2 \qquad (1)$$

where

$$\beta_P = K_P \frac{W_{M_P}}{2L_{M_P}}$$

and the drain current of M_N can be expressed as

$$I_{D(M_N)} = \beta_N \left(V_{in} - V_{SS} - V_{TN}\right)^2 \qquad (2)$$

where

$$\beta_N = K_N \frac{W_{M_N}}{2L_{M_N}}$$

Let $\beta_P = \beta_N = \beta$ by adjusting W_{M_P}/L_{M_P} and W_{M_N}/L_{M_N}, and assume that $V_{TN} = V_{TP} = V_T$, the output current of the V to I circuit can be obtained as

$$I_{out(V\,to\,I)} = I_{S(M_P)} - I_{D(M_N)}$$

$$= \left(\left(V_{DD} - V_T - V_{in}\right)^2 - \left(V_{in} - V_{SS} - V_T\right)^2\right)\beta$$

Setting $V_{SS} = -V_{DD}$ and the formula $(a+b)^2 - (a-b)^2 = 4ab$ is recognized, then $I_{out(V\ to\ I)}$ becomes

$$I_{out(V\ to\ I)} = -4V_{in}(V_{DD} - V_T)\beta \qquad (3)$$

The I to V circuit given by Wang [7] is shown in Fig.1b. It is composed of two NMOSs which are also biased in saturation region. The output voltage for $V_{SS} = -V_{DD}$ is given by

$$V_{out} = \frac{I_{in}}{2K_N \frac{W}{L}(V_{DD} - V_T)} \qquad (4)$$

The proposed adder circuit with three inputs is shown in Fig.2. It is composed of three V to I circuits and one I to V circuit. The components of the three V to I circuits are as follows: the first circuit consists of M_1 and M_4; the second circuit consists of M_2 and M_5; and the third circuit consists of M_3 and M_6. Note that the V to I circuits in the adder circuit have not the constant current sources since M_A and M_B in the I to V circuit are also operated as the constant current sources at the same time. The sum of the output currents of three V to I circuits can be written as

$$I_{out(sum)} = -4(V_1 + V_2 + V_3)(V_{DD} - V_T)\beta \qquad (5)$$

This sum of the output currents is the input current (I_{in}) of the I to V circuit which consists of M_A and M_B. After substitution of equation (5) into equation (4), the output voltage of the adder circuit can be written as

$$V_{out} = -(V_1 + V_2 + V_3) \qquad (6)$$

Note that the output voltage in this equation is the negative value. However, if the positive value of the output voltage is needed, this problem can be remedied using the positive output circuit in Fig.3 instead. From the circuit in Fig.3, two current mirrors and two constant current sources are added when compared with the circuit in Fig.2. Because $I_{out(sum)}$ converts the direction using two increased current mirrors, thus the output voltage of this adder circuit can be written as

$$V_{out} = V_1 + V_2 + V_3 \qquad (7)$$

3. Simulated Results

The proposed adder circuit in Fig.3 was simulated by the PSPICE program with the 0.8 μm level 3 MOS model. Two power supplies are V_{DD} = 1.5 V and V_{SS} = -1.5 V. The MOS sizes are (W/L) = 1.1 μm / 0.8 μm for all NMOSs and (W/L) = 2.9 μm / 0.8 μm for all PMOSs. The simulated output voltage, ideal output voltage, and the error between them when the input voltages: V_1 = 1 V, V_2 = -1 V to 1 V, and V_3 = -1 V are shown in Fig.4. It is evident in Fig.4 that the output voltage error is lower than 1 % when the range of V_2 from –500 mV to 275 mV is used. The operating frequency of the circuit up to 125 MHz by using the AC analysis when $V_1 = V_2$ = 200 mV and V_3 = -200 mV is shown in Fig.5.

4. Conclusions

A new CMOS adder has been designed, simulated, and described. The proposed adder circuit enjoys the following advantages:

(i) Few devices are employed when compared with the number of summing functions.
(ii) A narrow chip area is required because short channel MOSs are used.
(iii) The circuit consumes low voltage but has a wide output operating voltage range.
(iv) The circuit has wide operating frequency range.
(v) The next adder functions can be increased adding only two MOSs, one PMOS and one NMOS, per one next adder function.

5. Acknowledgment

This research was supported by the research support fund of the Ministry of University Affairs, Thailand.

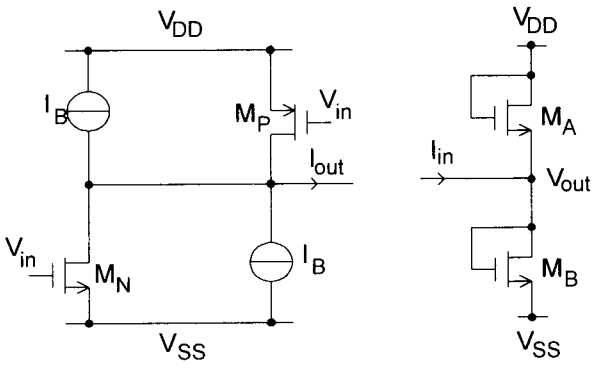

Fig.1 V to I and I to V circuits: a) Proposed V to I circuit and b) I to V circuit [7].

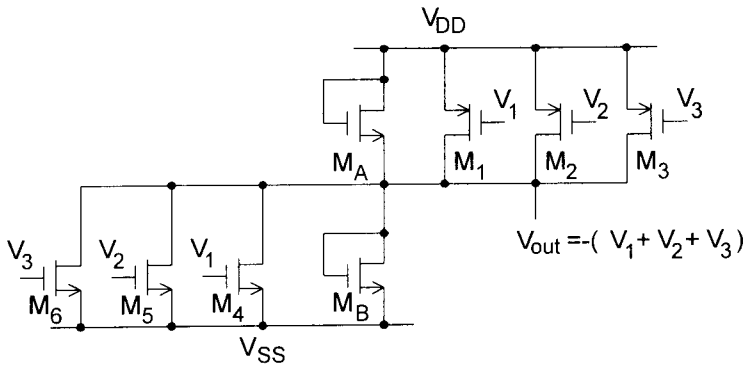

Fig.2 Proposed adder circuit.

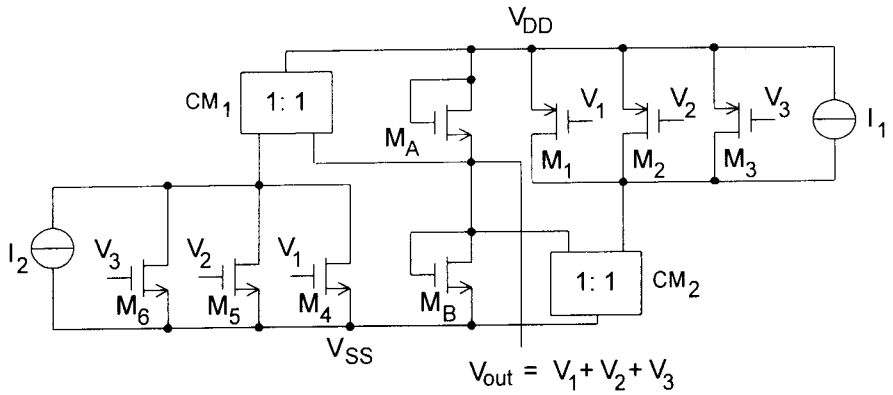

Fig.3 Proposed adder circuit with the positive value output voltage.

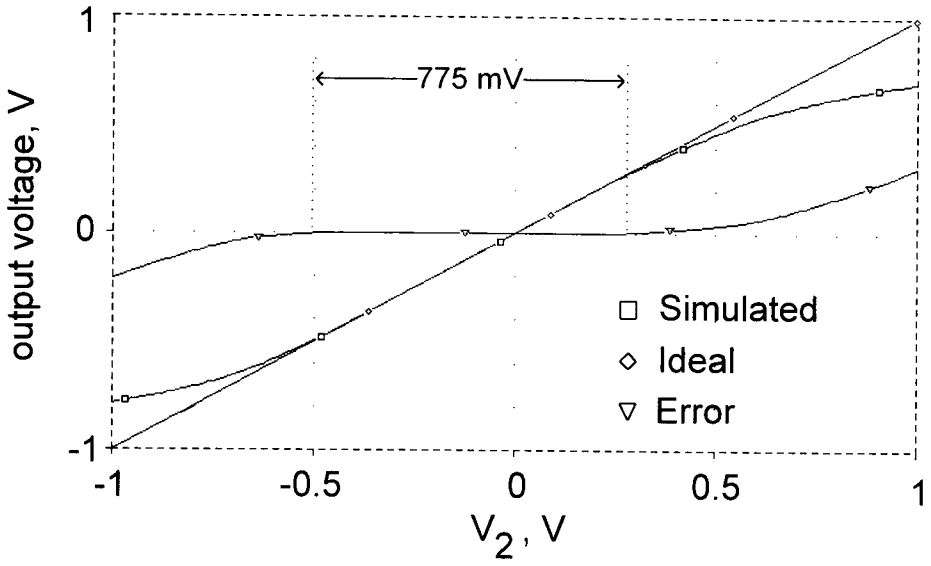

Fig.4 Relations between the input and output voltages.

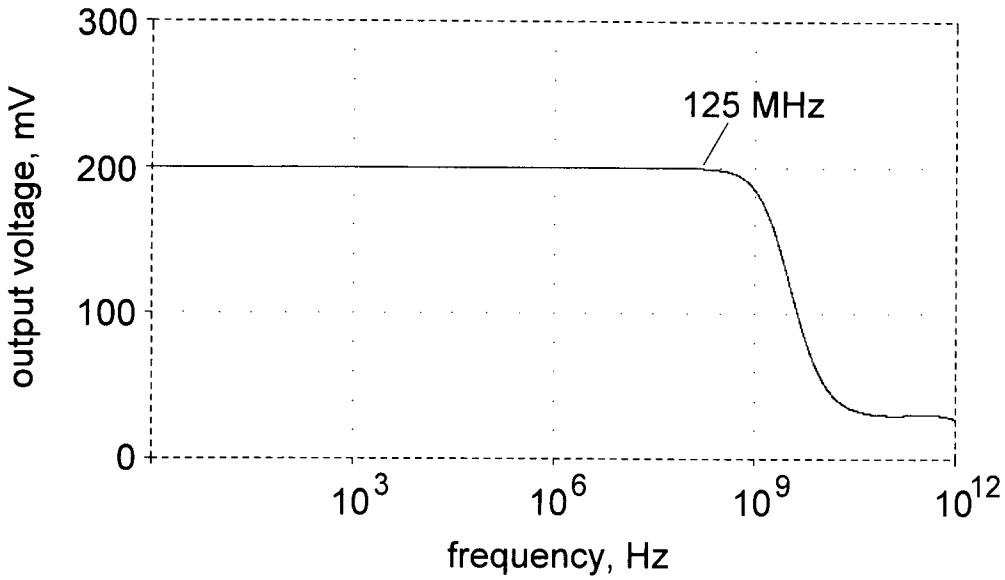

Fig.5 Simulated frequency response.

6. References

[1] Mead, C., Analog VLSI and Neural Systems, Addison-Wesley, New York, 1989.

[2] Ismail, M. and Fiez, T., Analog VLSI Signal and Information Processing, McGRAW-HILL, New York., 1994.

[3] Yamakawa, T., High-Speed Fuzzy Controller Hardware System: The Mega-FIPS Machine, Inform. Sci., Vol.45, pp.113-128, 1988.

[4] Tsay, S. W. And Newcomb, R., A Neuro-type Pool Arithmetic Unit, in Proc. IEEE, ISCAS'91 (Singapore), pp.2518-2521, 1991.

[5] Chaoui, H., CMOS Analogue Adder, Electron. Lett., Vol.31, pp.180-181, 1995.

[6] Fried, R. and Enz, C. C., Simple and Accurate Voltage Adder/Subtractor, Electron. Lett., Vol.33, pp. 944-945, 1997.

[7] Wang, Z., 2-MOSFET Transistors with Extremely Low Distortion for Output Reaching Supply Voltage, Electron. Lett., Vol.26, pp. 951-952, 1990.