A Fully-Balanced Wide-Frequency Current-Tunable Integrator

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Abstract

A new integrable fully-balanced wide-frequency current-tunable integrator is presented. The architecture of the circuit is relatively simple and symetrical with differential signals. The corner frequency is linearly tunable, through a bias current, over a wide-frequency sweep range of approximately three orders of magnitude. The maximum useful corner frequency is in excess of 75 MHz.

1. Introduction

Integrators are needed in many applications such as in sinusoidal quadrature oscillators used in a digital modulator of an integrated receiver. It is usually desirable that the architecture of such devices is fully balanced with differential signals so as to enable, for example, accurate quadrature outputs with maximum symmetry over a wide tunable-frequency sweep range. There are other significant, well understood advantages in employing a fully balanced realisation [1]. Several techniques of such integrators have been suggested [2-5].

In this paper, a relatively simple circuit technique to realise an integrable fully-balanced wide-frequency current-tunable integrator is presented. The architecture of the circuit is relatively simple and symetrical with differential signals. The corner frequency of the integrator is linearly current-tunable using a tunable r_e network where r_e is the small-signal dynamic resistance of a forward biased base-emitter junction of a bipolar transistor.

2. Circuit Descriptions

Figure 1 shows the basic circuit configuration of the fully-balanced current-tunable integrator consisting of eight matched npn transistors Q1 to Q8, a capacitor C and two identical current sinks of value I_f. The differential, small-signal, input voltage V_{in} is applied to the bases of the differential pair Q1 and Q2, between points A and B, and the differential, small-signal, output voltage V_o is taken across the emitters of Q6 and Q5, between points D and E. The corner frequency ω_0 of the integrator, typically defined at the point where the magnitude and the phase shift of its transfer function V_o/V_{in} become 0 dB and -90 degrees, respectively, is tunable using a current-tunable loading resistance $R = 4r_e$, formed by Q5, Q6, Q7 and Q8.

The two current sinks may be implemented through the conventional Wilson current mirrors and convert a frequency setting current I_f to bias Q5, Q6, Q7 and Q8, as well as current $I_f / 2$ to bias Q1, Q2, Q3 and Q4. It can be seen from Figure 1 that the architecture of the circuit is symetrical and hence the name "fully-balanced" integrator. The circuit is also relatively simple and is "integrable" as all active devices can be fabricated on-chip.

3. Ideal Analysis

Referring to Figure 1, assuming that the collectors of Q3 and Q4, and the bases of Q4 and Q3, are temporarily disconnected with points E and D, and that the bias currents of Q5

to Q8 remain I_f whilst the bias currents of Q1 and Q2 remain I_f / 2. In such a temporary case, let the small-signal input voltage across points A and B be V'_{in} and the resulting small-signal output voltage across points D and E be V'_o. The small-signal input voltage V'_{in} results in a differential output current i_{dl} through the loading impedance Z between points D and E where

$$Z = \frac{R}{(1 + s\tau)} \qquad (1)$$

$$\tau = CR = \left(\frac{4CV_T}{I_f}\right) \qquad (2)$$

and V_T is the usual thermal voltage associated with a pn junction and is approximately equal to 25 mV at room temperature. The transfer function V'_o/V'_{in} therefore represents a low-pass filter of the form

$$\frac{V'_o}{V'_{in}} = \frac{1}{(1 + s\tau)} \qquad (3)$$

Such a low-pass filter will be referred to as the 1st low-pass filter.

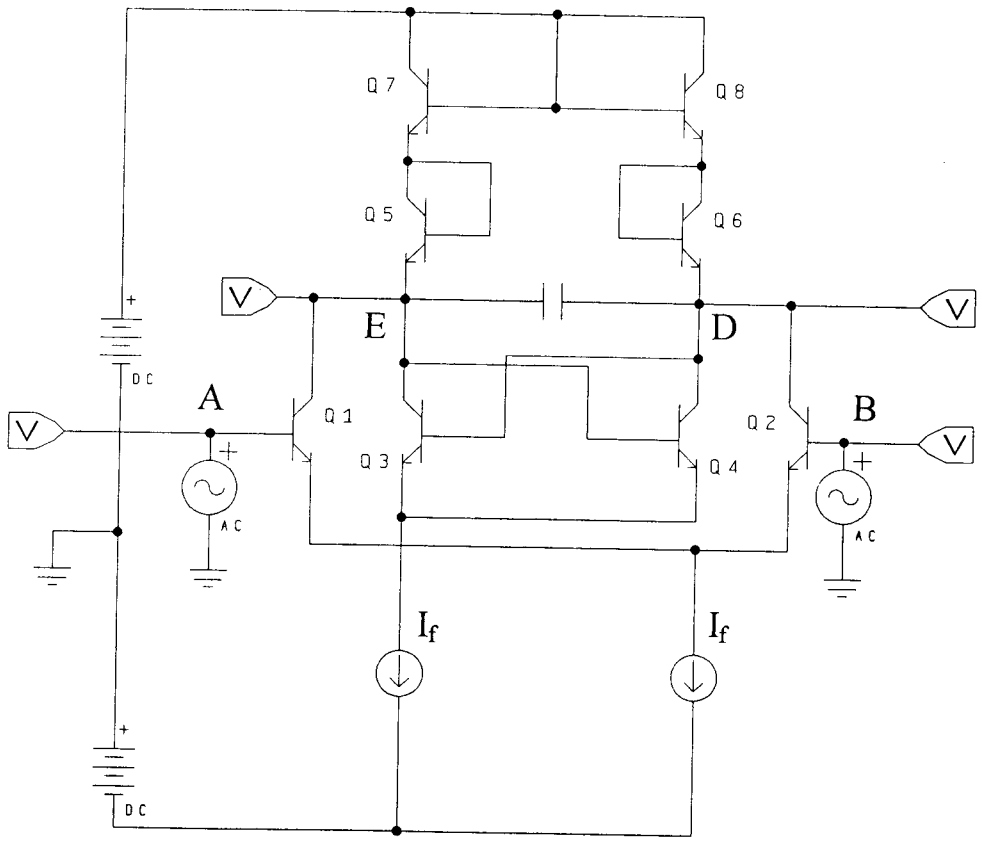

Figure 1 : Schematic diagram of the fully balanced wide-frequency current-tunable integrator.

By reconnecting the collectors of Q3 and Q4 (the bases of Q4 and Q3 remain disconnected) with points E and D, let us assume similarly that the collectors of the differential pair Q1 and Q2 are temporarily disconnected with points E and D, and that the bias currents of Q5 to Q8 remain I_f whilst the bias currents of Q3 and Q4 remain $I_f / 2$.

The small-signal input voltage V^*_{in} is applied to the bases of Q3 and Q4 resulting in a differential output current i_{d2} through the loading impedance Z shown in equation (1). The small-signal output voltage V^*_o is taken across points D and E. One can show that the transfer function V^*_o/V^*_{in}, also represents a low-pass filter of the similar form shown in equation (3). Such a low-pass filter will be referred to as the 2nd low-pass filter.

With reference to Figure 1 (with the connection as shown), the differential output current i_{d1} obtained from the 1st low-pass filter is added together with the differential output current i_{d2} obtained from the 2nd low-pass filter. In other words, the loading impedance Z is acting as a current adder. Note that the resulting differential output voltage V_o (across Z) becomes the differential input voltage to the 2nd low-pass filter. One can therefore show that the overall transfer function V_o/V_{in} is of the form

$$\frac{V_o}{V_{in}} = \frac{1}{(1 + s\tau)} \times \frac{(1 + s\tau)}{s\tau} \qquad (4)$$

$$= \frac{1}{s\tau} \qquad (5)$$

It can be seen that equation (5) represents the transfer function of a 1st-order integrator. The corner frequency ω_0 of such an integrator is of the form $\omega_0 = \frac{1}{\tau} = \frac{I_f}{4CV_T}$ (6)

It can be seen from equation (6) that the corner frequency ω_0 is tunable through the bias current I_f and hence the name "current-tunable integrator".

4. Simulation Results

The performance of the circuit shown in Figure 1 has been simulated using a circuit simulator package ViewSpice [6], running on a 32-bit personal computer. The npn transistors are modeled by QMPS2222A, whose transition frequency f_T is at 300 MHz [6]. Figure 2 illustrates magnitude (dB) and phase shift (degrees) of V_o/V_{in} versus frequency (Hz) obtained from the simulation using, for example, capacitor C = 0.01 μF and I_f = 7 μA, 70 μA, 0.7 mA and 7 mA.

It can be seen from Figure 2 that the corresponding corner frequencies ω_0, where the magnitude of V_o/V_{in} becomes 0 dB, for individual values of I_f are at 1.067 kHz, 10.67 kHz, 106.7 kHz and 1.06 MHz, respectively, and the corresponding phase shifts for individual values of I_f are all approximately -89 degrees.

Figure 3 depicts the simulation results of both the corner frequencies (Hz) and the corresponding phase shift (degrees) of V_o/V_{in}, where the magnitude of V_o/V_{in} becomes 0 dB, versus the bias current I_f (A), using a fixed capacitor C of value 0.01 μF. For purposes of comparison, the ideal (expected) results are also included. It can be seen from Figure 3 that both the expected and the simulated results are consistent, and the corner frequency is linearly current-tunable over a "wide-frequency" sweep range of approximately 3 orders of magnitude.

Figure 4 shows the simulation results of both the corner frequencies (Hz) and the corresponding phase shift (degrees) of V_o/V_{in}, where the magnitude of V_o/V_{in} becomes 0 dB, versus the capacitance C, using a fixed bias current I_f of value 2 mA. For purposes of comparison, the ideal (expected) results are also included. It can also be seen from Figure 4 that both the expected and the simulated results are linear and consistent and, by using a minimum frequency setting capacitance of 20 pF, the upper frequency limit can be expected to be 75 MHz.

5. Discussion and Conclusions

A new integrable fully-balanced wide-frequency current-tunable integrator has been presented. The architecture of the circuit is symetrical with differential signals. The circuit is also relatively simple and integrable on-chip. Both the simulated and the ideal results are consistent. The corner frequency is linearly current-tunable over a wide-frequency sweep range of three orders of magnitude. The maximum useful corner frequency is around 75 MHz. By using better transistors of much higher f_T (e.g. in the region of several GHz) and much smaller value of C (e.g. using stray capacitance), much higher values of the corner frequency, as suggested by equation (6), could be expected.

References

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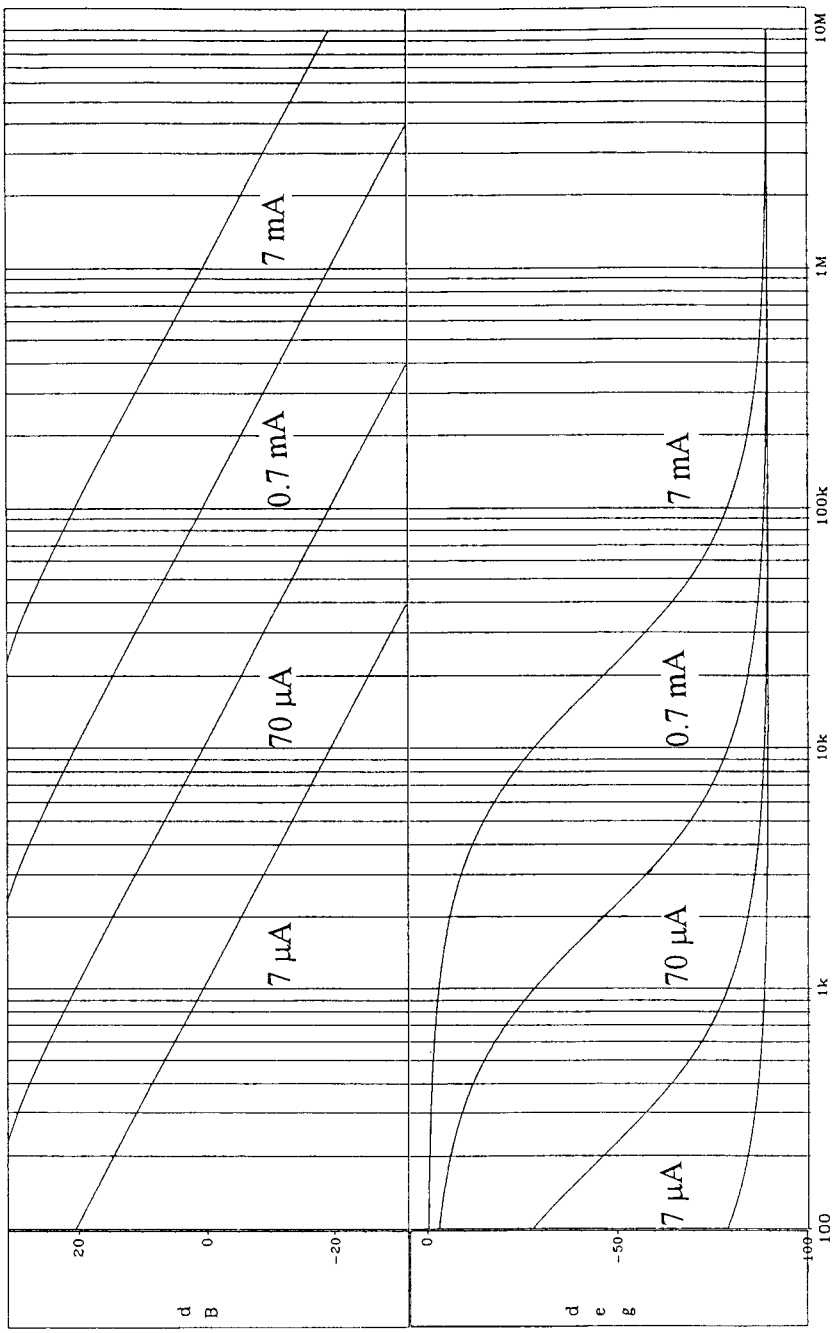

Figure 2 : Magnitude (dB) and phase shift (degree) of V_0/V_{in} versus frequency (Hz) using the capacitor C = 0.01 µF and the bias current I_F = 7 µA, 70 µA, 0.7 mA and 7 mA.

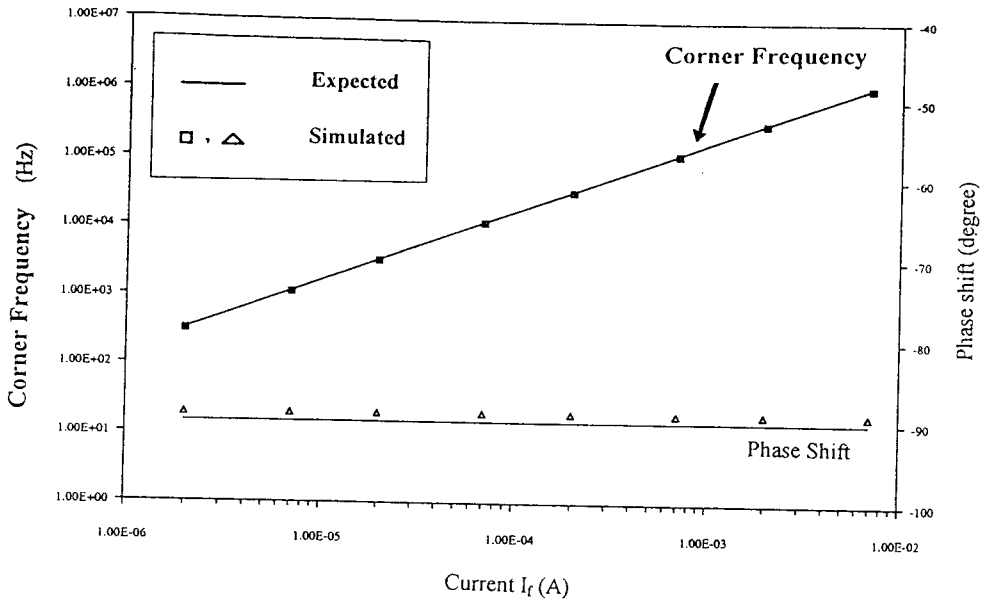

Figure 3 : Corner frequencies (Hz) and the corresponding phase shift (degree) of V_0/V_{in} versus the bias current I_f (A), using a fixed capacitance C of value 0.01 μF.

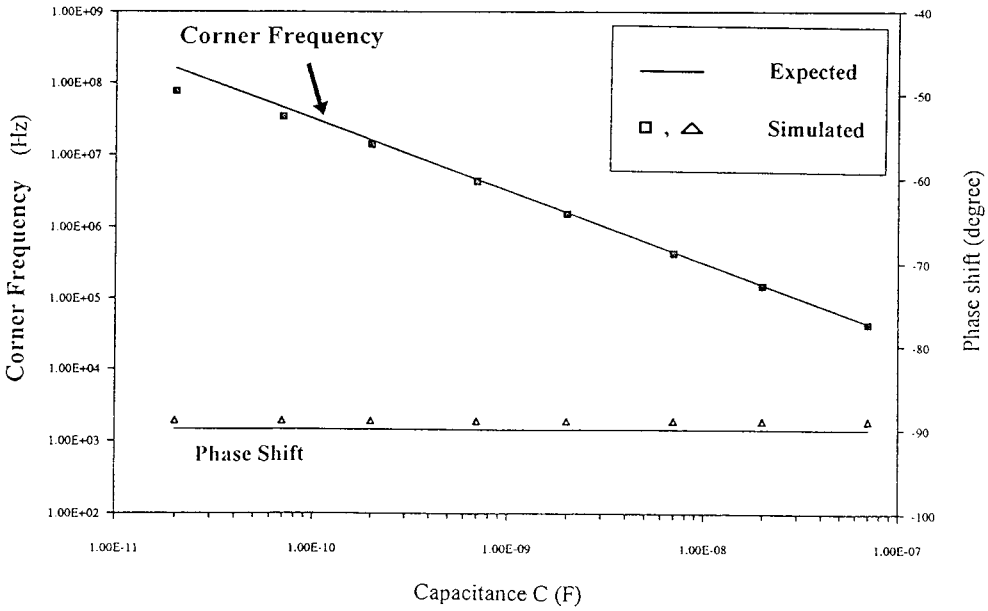

Figure 4 : Corner frequencies (Hz) and the corresponding phase shift (degree) of V_0/V_{in} versus the capacitance C (F), using a fixed bias current I_f of value 2mA.