Floating Capacitance Multiplier Using DVCC and CCCIIs

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บทคัดย่อ

บทความวิจัยนี้ นำเสนอวงจรคูณค่าความจุแบบลอยโดยใช้ DVCC ร่วมกับวงจรสายพานกระแสรุ่นที่สองที่ควบคุมได้ด้วยวิธีการทางอิเล็กทรอนิกส์วงจรที่นำเสนอเป็นการสังเคราะห์ตัวเก็บประจุแบบลอยโดยใช้ตัวเก็บประจุที่ถูกต่อลงกราวด์ จุดเด่นของวงจรที่นำเสนอคือสามารถปรับค่าความจุได้ด้วยวิธีการทางอิเล็กทรอนิกส์ การทำงานของวงจรเป็นอิสระจากการเปลี่ยนแปลงของอุณหภูมิผล การจำลองด้วยโปรแกรม PSPICE พบว่าการทำงานวงจรที่นำเสนอเป็นไปตามที่คาดการณ์ไว้ นอกจากนี้ยังได้ นำเสนอวิธีการเพิ่มค่าความจุในวงจรและตัวอย่างการนำไปใช้งานวงจรกรองความถี่สูงลำดับห้าของ Chebyshev

Abstract

This article introduces a floating capacitance multiplier employing differential voltage current conveyor (DVCC) and second generation current controlled current conveyors (CCCIIs). The provided capacitor is a floating element synthesized from a grounded capacitor. Its outstanding features are that the capacitive value can be adjusted by input bias currents of the CCCIIs and is theoretically temperature-insensitive. The circuit construction comprises one DVCC and two CCCIIs, cooperating with a grounded capacitor. The circuit performances are depicted through PSPICE simulations, they show good agreement to theoretical anticipation. Capacitance increasing technique and an application as a fifth-order Chebyshev high-pass filter are included.

1. Introduction

It is well accepted that a capacitor is an important element which is used in the most of circuits and systems. For example, it is used for tuning in filters, oscillators and etc. However, in the integrated circuit fabrication, it is impractical to realize large-valued capacitors because of the occupied area. In fact, in a standard CMOS polysilicon layers, a 20pF capacitor is equivalent, relatively to the silicon area, to thousands of transistors [1]. This means that the integration of capacitor as large as 100pF is not possible. In some applications, however, such as integrated lock-in amplifiers, sampled-data systems and capacitive sensor interfaces [2-5], they are necessary to have higher capacitive values.

A possible solution is the use of a capacitance multiplier, which performs the multiplication of small capacitive values, to obtain higher equivalent integrated capacitors, avoiding the need of a large silicon area [6]. From literature studies, several works which can provide a multiplied capacitor have been proposed. Although, the voltage-mode operational amplifier (op-amp) based capacitance multipliers are available in the literatures [7-9], they are not suitable from the view point of IC fabrication.

The modern active building blocks employ to synthesize the capacitance multipliers are emphasized on Operational Transconductance Amplifiers (OTAs) [9-11] and current conveyors [12-18] due to commercial availabilities. The literature surveys show that a

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large number of modern circuit realizations for capacitance multipliers have been reported [10-18]. Unfortunately, these reported circuits suffer from one or more of following weaknesses;

a) need for passive element matching [9-11, 15-16],

b) lack of electronic tunability [12-15,17], which can not be implemented in automatic control systems,

c) excessive use of the active and/or passive elements [10-18],

d) use of floating capacitor, which is not convenient to further fabricate in IC [9-11, 13, 17],

e) providing only a grounded capacitor, which offer applications less than a floating capacitor [11-13, 17],

f) use of a capacitor connected to inappropriate terminal, which results in an extra pole, and consequently lower frequency of operation [12, 18]

A major restriction of the all previous capacitance multipliers is temperature dependence of the capacitive values due to parasitic parameters of active elements used in circuits which limits the performances of the circuits, especially in the works suffered from environment variations.

In this paper, we present a novel capacitance multiplier emphasizing on use of the DVCC and CCCIIs. The features of proposed circuit are that: the proposed circuits consume a few number of active element: it employs only single grounded capacitor, which is convenient to realize in IC [19-20]: it does not need any matching conditions of the elements: it can used over a wide range of frequency because of capacitor connected to high output impedance of DVCC, then it does not generate an extra pole which restricts operation frequencies: especially, the capacitive value is temperature-insensitive. In addition, it can be controlled via input bias currents. The performances of proposed circuit are illustrated by PSPICE simulations, they show good agreement as depicted. Capacitance increasing and an application as a fifth-order Chebyshev high-pass filter are included.

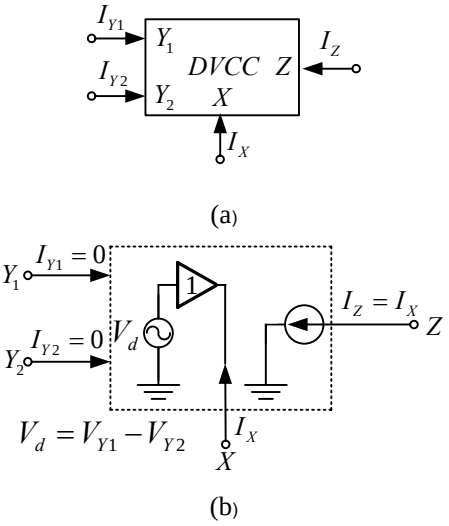


Figure 1 DVCC (a) Symbol (b) Equivalent circuit**.**

2. Principle of Operation

2.1 The Differential Voltage Current Conveyor (DVCC)

The DVCC, whose electrical symbol and equivalent circuit are shown in Figure. 1, is a four-terminal network with the terminal ideal characteristics described by following equation

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y1} \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{bmatrix}. \quad (1)$$

2.2 The Second Generation Current Controlled Current Conveyor (CCCII)

The characteristics of ideal CCCII are represented by the following hybrid matrix

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (2)$$

Where the positive and negative signs define a positive and negative current controlled current conveyor (CCCII+, CCCII-), respectively. The intrinsic X terminal current controlled resistance is given as

$$R_x = \frac{V_T}{2I_B} \quad (3)$$

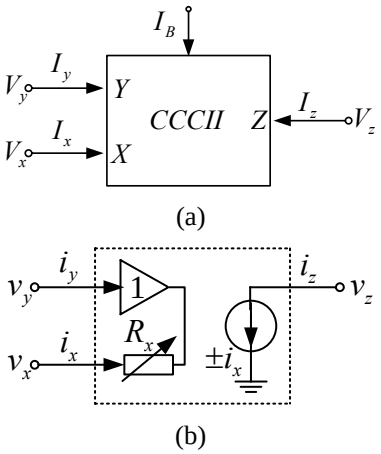


Figure 2 The CCCII (a) Symbol (b) Equivalent circuit.

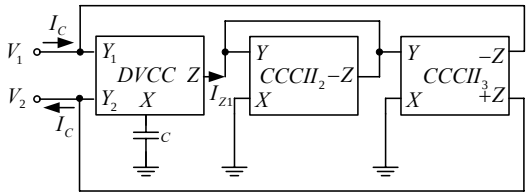


Figure 3 Proposed floating capacitance multiplier.

Where I_B and V_T are bias current and thermal voltage, respectively. The symbol and the equivalent circuit of the CCCII are illustrated in Figure 2(a) and (b), respectively.

2.3 Proposed Capacitance Multiplier

Figure 3 depicts the proposed floating capacitance multiplier. Considering the circuit in Figure 3 and using DVCC and CCCII properties in section 2.1 and 2.2, we will receive

$$I_{Z1} = sC(V_1 - V_2) \tag{4}$$

Then, input current of the circuit is given by

$$I_C = I_{Z1}\frac{R_{X2}}{R_{X3}} \tag{5}$$

Summarily, the input impedance of the proposed circuit can be found as

$$Z_{in} = \frac{V_1 - V_2}{I_C} = \frac{R_{X3}}{sCR_{X2}} \tag{6}$$

From Eqn. (6), it is clearly seen that, the proposed circuit can provide the new floating capacitor with a value

$$C_k = \frac{R_{X2}C}{R_{X3}} \tag{7}$$

If we substitute $R_{Xi} = V_T / 2I_{Bi}$, the floating capacitance is modified to

$$C_k = K_{mul}C = \frac{I_{B3}}{I_{B2}}C \tag{8}$$

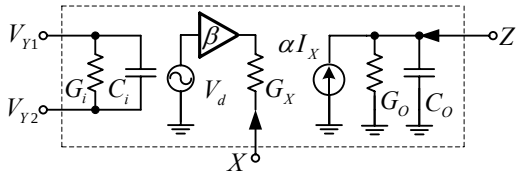
It is evident that, the capacitive value is multiplied with a gain

$$K_{mul} = \frac{I_{B3}}{I_{B2}} \tag{9}$$

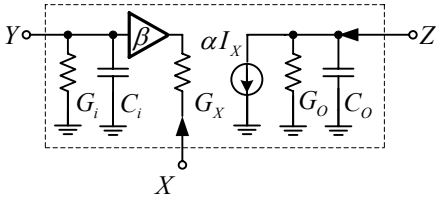
We can found that, if the connected capacitor is free from temperature, the capacitive value is temperature-insensitive and can be adjusted by any input bias currents.

2.4 High Frequency Consideration

At high frequency application, the parasitic elements affect the frequency response of the proposed



(a)



(b)

Figure 4 Circuit model with parasitic elements of (a) DVCC (b) CCCII.

circuit. The equivalent circuit of DVCC and CCCII with the parasitic elements can be seen in Figure 4, where C_i, C_o and R_o are input, output stray capacitances and finite output resistance of DVCC and CCCII, respectively.

By straightforward analysis using circuit model from Figure 4 and considering the circuit from Figure 3, we will receive

$$Z_{in} = \frac{(G_B + sC_B)(1 + \alpha_2\beta_2 G_{X2}(G_A + sC_A))}{\left((1 + \alpha_2\beta_2 G_{X2}(G_A + sC_A)) + \alpha_1\beta_1\alpha_3\beta_3 G_{X3}(G_A + sC_A)(G_{X1} + sC)(G_B + sC_B)\right)} \quad (10)$$

Where

$C_A = C_{O1} + C_{O2} + C_{i2} + C_{i3}, G_A = G_{O1} + G_{O2} + G_{i2} + G_{i3}, G_B = G_{O3} + G_{i1}$ and $C_B = C_{O3} + C_{i1}$

2.5 Principle of Capacitance Increasing

Figure 5 gives the theoretical implementation of the high-value controlled. The output stage of circuit in Figure 3 is constituted by a dual output current amplifier. Then, the output currents of current amplifier are equal to $|I_0| = nI_{Z3}$. So, the input impedance of circuit in Figure 5 becomes

$$Z_{in} = \frac{V_1 - V_2}{I_C} = \frac{R_{X3}}{nsCR_{X2}} \quad (11)$$

It is evident that, the capacitive value is multiplied with a gain

$$K_{mul} = \frac{nI_{B3}}{I_{B2}} \quad (12)$$

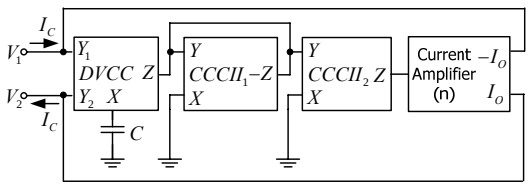


Figure 5 Symbolic implementation of the controlled capacitance.

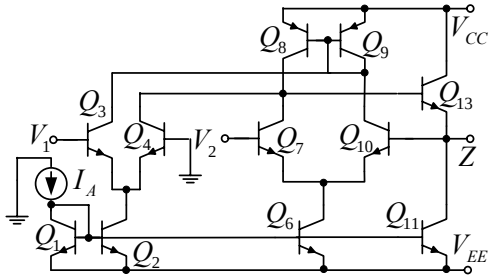


Figure 6 Internal construction of DVCC.

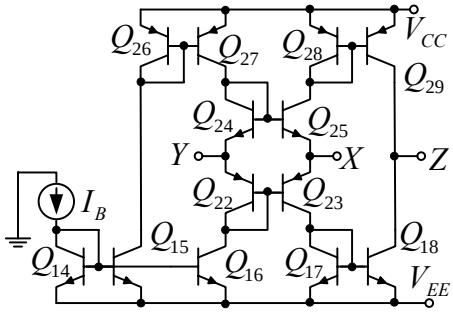


Figure 7 Internal construction of CCCII.

From Eqn. (12), it is clearly seen that, we can control the capacitive value by adjusting the current gain of the current amplifier circuit.

3. Simulation Results and Discussions

To prove the performances of the proposed circuit, the PSPICE simulation program was used for the examination. The PNP and NPN transistors employed in the proposed circuit were simulated by respectively using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T [21] with ±1.5V supply voltages. Figure 6 and 7 depict respectively schematic description of the DVCC and CCCII used in the simulations.

To illustrate frequency response of the floating capacitance multiplier, Figure 8 shows the phase and magnitude of input impedance for several frequencies. It should be noted that the usable frequency range of the proposed circuit is up to approximately 3MHz. At higher frequencies, the internal parasitic elements, covering capacitances and resistance as explained in Section 2.4, degrade the performances of the proposed circuit. Similarly, these factors effect on temperature

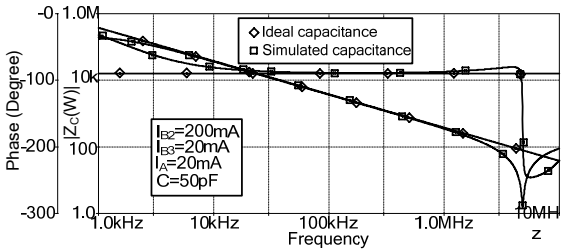


Figure 8 Phase and Magnitude of input impedance relative to frequency variations.

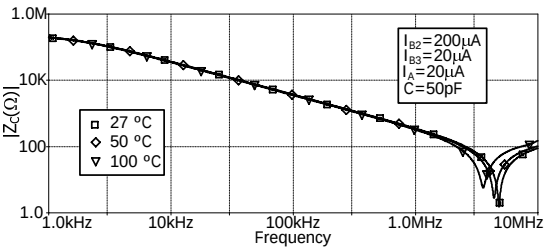


Figure 9 Frequency responses of magnitude of input impedance due to temperature variations.

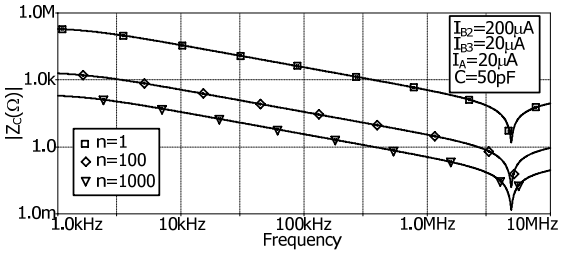


Figure 10 Magnitude of input impedance relative to frequency variations of circuit in Figure.5.

dependence of input impedance at the higher frequencies, as shown in Figure 9.

In addition, from the result in Figure 9, it is insisted that in the usable frequency range, the proposed circuit provides a floating capacitance with temperature-insensitive. Figure 10 shows the magnitude of input impedance relative to frequency variations of circuit in Figure 5. The ideal current amplifier is used for the simulation.

To show usability of the proposed circuit, an application as a fifth-order Chebyshev high-pass filter [22] as shown in Figure 11 is included. The results of frequency responses of the proposed capacitance

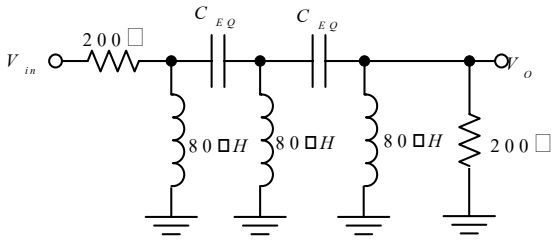


Figure 11 A fifth-order Chebyshev high-pass filter.

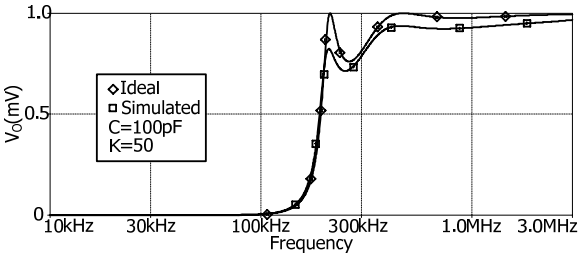


Figure 12 Frequency responses of the circuit in Figure 11.

multiplier, compared to the ideal capacitance, are confirmed in Figure 12. Where $V_{in} = 2mV$

4. Conclusion

A novel floating capacitance multiplier using DVCC and CCCIIs has been introduced in this paper. The capacitive value can be widely adjusted by any input bias currents of the CCCIIs and is temperature-insensitive. The circuit construction comprises only three active elements, cooperating with a grounded capacitor. The PSPICE results confirm the mentioned benefits. The power consumption is approximately 2.32mW at ±1.5V supply voltages. Consequently, the proposed floating capacitance multiplier is appropriate for and further fabricating into an integrated circuit and implementing to capacitance-based circuits**.** Capacitance increasing and an application as a fifth-order Chebyshev high-pass filter are included.

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