Research Article

Behavior of Ta_2O_5-Si Capacitors with Different Gate Electrode under Constant Current Stress

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Abstract

The electrical characteristics of MOS capacitors with Ta_2O_5 as oxide and with different gate electrodes (Al, Au, W, TiN) are investigated using high frequency capacitance-voltage (*C-V*) and current–voltage (*I-V*) measurements. The influence of deposition techniques of gate electrode (reactive sputtering and evaporation) and the type of electrode material (different work functions) are observed. Charged trapping properties were studied by measuring the gate voltage shift due to trapped charge generation in order to investigate the response to constant current stress (CCS) under various current/time conditions at room temperature. The results showed that the presence of pre-existing electron traps leads the changes of time dependent voltage during gate injected CCS in the initial stage, followed by the slow positive charge build-up, same for all the structures and characteristic for this oxide. Gate-induced defects due to ther rate of reaction of gate electrode with the oxide are responsible for different behavior of the structures with different gate electrodes, observed in the initial stage of CCS. The Au-gated devices appear to be the most susceptible to the constant current stress degradation. They also have highest values of capacitance and lowest leakage currents.

Key Words: Gate electrode; Dielectric properties; Oxides; Constant current stress

Introduction

For few decades, the semiconductor industry used silicon dioxide as its gate insulator. SiO_2, with a dielectric constant of 4.2, is well investigated, its electrical characteristics are known and it is highly compatible with the transistor's underlying silicon metal layer. The rapid shrinking of transistor feature sizes has resulted in shrinking semiconductor size, according to Moore's law. The SiO_2 transistor gate thickness needed to decrease to maintain adequate capacitance across it, but below 2 nm, the gate oxide becomes so thin that direct tunneling currents through it rapidly increase and make this oxide unsuitable for further use in microelectronics industry.

Logical solution of this problem is to replace poly silicon gates and silicon oxide with metal gates and alternative high-k gate dielectrics. These

materials have the same value of capacitance at greater physical thickness, thus avoiding tunneling effect. But, several points are to be fulfilled. High dielectric constant, low leakage current, low dielectric loss, high breakdown voltage, good interface and thermal stability sufficient to resist the high temperature CMOS manufacturing processing are required. Necessity of new gate dielectric materials with higher dielectric constant *k*, (in the interval 10-100) such as Ta_2O_5, TiO_2, Y_2O_3, HfO_2, Er_2O_3 Al_2O_3, CeO_2, ZrO_2, La_2O_3 and Nb_2O_5 as a replacement for currently dominant SiO_2 appeared (Brown, 2004). These materials can be deposited with several methods compatible with existing industrial production including chemical vapor deposition (CVD), and its variations like metalorganic chemical vapor deposition (MOCVD), anodization, DC sputtering, reactive magnetron sputtering, atomic layer deposition (ALD) etc. (Groner and George, 2003).Their characteristics are intensively studied now days in order to integrate in future generations of integrated circuits (Atanassova and Paskaleva, 2007).

Other materials with even higher value of dielectric constant are perovskite materials. They have tendency to have very large dielectric constants due to their ferroelectric behavior at temperatures below the Curie point (Wilk, 2001; Groner and George, 2003). Barium titanate ($BaTiO_3$) based ceramics with the perovskite structure can exhibit relative dielectric constant as high as 15000 (Swartz, 1990), depending on the grain size and crystal structure. Other perovskite material with high dielectric constant is $SrTiO_3$ (Vehkamaki, 2001). Higher dielectric constant $k \sim 10^3$-10^4 is obtained with mixing these two materials to form $Ba_xSr_{1-x}TiO_3$ (BST) (Kingon, 2000). BST has been used in bulk capacitors and is being investigated for DRAM capacitor applications. Even higher dielectric constants $k > 10^4$ have been achieved by doping high-*k* perovskites materials (Nalwa, 1999). Such ceramics have a face-centered-cubic crystal structure and no net polarization of charge above their Curie point. Below this temperature, the ions shift to create a permanent dipole in the material and exhibit a very high dielectric constant. But, there is some indication that the dielectric constant of perovskites decreases for thin films with thicknesses <1nm, where the crystal structures responsible for the high-*k* values are no longer present in thin films (Kingon, 2000). This lack of scalability will restrict the application of perovskites to devices with thicker dielectric films. This lack of scalability may mean that perovskites do not have an advantage over other high-*k* materials for memory and logic applications. Problems may also arise due to the low Curie temperature of some of these perovskite materials. The lower Curie temperature will make these materials unsuitable for devices with high operating temperatures.

Silicon gates are also replacing with new materials for gate electrodes. Few parameters are to be observed in finding the most appropriate candidate for this role. Very important characteristics of these materials are their work function, resistivity and compatibility with the existing semiconductor processes (Jiang and Chen, 2004). Some of those materials that reach the demands for gate application in MOS systems are Al, Au, W, TiN, W/TiN (Lee et al, 2001; Gilmer et al., 2000), WN, and TaN (Lee et al, 2000).

In this article we investigated Ta_2O_5 as a gate dielectric. This material showed itself as a potential replacement for SiO_2 because of its ability for deposition by conventional methods with equipment already available in process line, high capacitance per unit area and low leakage current density. (ITRS) With these characteristics, tantalum pentoxide

appeared appropriate for applications in high-density dynamic-random-access memories (DRAMs). Its dielectric and electric behavior with Al as gate electrode were already subjects of investigation (Atanassova et al., 2002; Pecovska-Gjorgjevich et al., 2003; Novkovski et al., 1999). The conduction mechanism in Ta_2O_5 in low voltage range within the devices that work nowadays and the gate oxide reliability is studied extensively. The results from our earlier works (Pecovska-Gjorgjevich et al, 2004; Pecovska-Gjorgjevich et al., 2005) showed that Schottky emission (electrode limited emission) was dominant conduction mechanism for low fields and Pool-Frenkel mechanism, normal or modified (bulk limited with high concentration of defects), appeared at medium fields.

In order to define the most appropriate gate material for its improved performance, structural and dielectrics properties and degradation of gate/Ta_2O_5/Si capacitors with different material gate electrodes under constant voltage stress were investigated earlier, (Spassov et al., 2006; Atanassova et al., 2008; Novkovski and Atanassova, 2005). Changing the gate material, i.e. the work function between the metal gate and the poly-Si substrate, we observed the difference in the leakage currents and the possible improvement of the MOS structures.

In our work we investigated the electrical characteristics (*C-V* and *I-V*) of the structures from the aspect of different gate electrodes. We submitted these structures to constant current stress and discussed their behavior. The materials used for the gate electrode were Al, Au, W and TiN.

Materials and Methods

Tantalum pentoxide thin films were deposited on p-type Si substrates (15-17Ωcm) by reactive sputtering of Ta-target in an Ar/O_2 mixture (O_2 content N_c=10%, substrate temperature T_s = 493K). Thicknesses of the films measured by ellipsometry with laser light of λ = 632.8 nm are ~17 nm. MOS structures were formed with evaporation of Au or Al layer as a gate; and by reactive sputtering of W or TiN (gas pressure 3 Pa, rf power density 3 W/cm^2). The sample preparation and its structure investigations can be found elsewhere (Atanassova and Spassov, 1999; Atanassova et al., 2002; Atanassova and Spassov, 2000). The gate areas were $1.96 \cdot 10^{-3}$cm^2 for Au and $2.5 \cdot 10^{-3}$cm^2 for Al, W and TiN. Because of its thermodynamic activity Si substrate reacts with Ta_2O_5 which results in reducing the oxide film and forming an interfacial layer of SiO_2 (or SiO_x, or SiTaO layer). This interface layer induces defects that increase leakage currents and lead to higher interface state density and lower breakdown strength (Lai et al., 2002). Interfacial layers can severely decrease the capacitance of a high-*k* film. The equivalent SiO_2 thickness of the MOS structure is increased and the capacitance of Ta_2O_5 is calculated from the structure formed of two serial capacitors (first the layer of SiO_2 and the second the layer of Ta_2O_5).

Thin interlayer of SiO_2 ~3 nm between Si substrate and the Ta_2O_5 dielectric is formed in our structures (Atanassova et al., 2002; Atanassova and Spassov, 1999; Atanassova et al., 1995; Dimitrova et al., 2001) which generates a lot of traps and puts this material appropriate for memory application. It is well known that memory capacitors require extremely low leakage currents ($<10^{-8}$A/cm^2) at low electric field and high capacitance density, for charge storage, but the interface quality is not as critical to capacitor performance (Wilk et al., 2001). In order to decrease the negative charge density in the structures (to repair oxygen vacancies and various structural non-perfections present in the as-deposited films) and obtain better thermal stability, all films are submitted to a H_2 post

metallization annealing at 450˚C for one hour.

Typical *I-V* curves for both gate polarities were made with HP 4140B picoammeter with voltage step of 0.1 V and rate of 0.1 V/s with a delay time of 2.5 s before recording the current. The negative bias (electron injection is from the gate electrode) refers to Si-substrate in accumulation and the positive bias (electron injection from the substrate) to Si-substrate in inversion.

In order to investigate the electric/defect characteristics of the structures, high frequency capacitance-voltage (*C-V*) measurements were carried out by HP LCR meter at 1MHz with a step of 10 mV.

Time dependence of the gate voltage was investigated performing constant current stress measurements with low-high current gate injection using HP 3458A multimeter. The stressing was biased negatively, with current injection from the gate, i.e. p-Si substrate in accumulation.

All measurements were performed at room temperature.

Results and Discussion

Typical *I*-V characteristics for all structures for gate positive and negative biased are shown in Figure 1. Leakage current density for all samples is bellow 10^{-7} A/cm^2 untill 1.7-2.9 MV/cm (3-5V) for negative bias and 0.9-1.7 MV/cm (1.5-3V) for positive bias. The gate current depends on the barrier height and on the position of the potential maximum in the dielectric near the injection contact. The characteristics are sensitive to the internal field and the space charge in the oxide which, in turn, affects the barrier height and the position of the potential maximum near the interface (NANDI et al., 2003). Higher leakage currents under positive bias come from the presence of the SiO_2 interface layer between Si substrate and Ta_2O_5 which defines

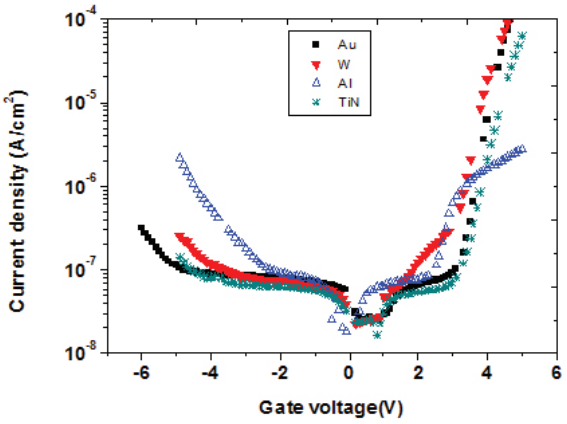

Figure 1 Leakage current density for rf sputtered Ta_2O_5 films with different gate electrodes

the leakage current and the conduction is limited by electron injection into SiO_2 from the Si (Nishioka et al., 1987). The results giving leakage current density bellow 10^{-7} A/cm^2 at ±1V for all structures are similar with the literature (Liu et al., 2011).

The leakage currents of the structures were observed in Schottky emission term (SE electrode limited conduction) given with $\ln J \ vs \left(E^{1/2}\right)$ dependence, Pool-Frenkel term (PF bulk limited conduction), defined with $\ln\left(\frac{J}{E}\right) \ vs \ \left(E^{1/2}\right)$ and Fowler-Nordheim tunneling effect, described as $\ln\left(\frac{J}{E^2}\right) \ vs \ \left(\frac{1}{E}\right)$.

In accumulation regime, (negative bias) Schotky emission dominates for low fields (till 1.5 MV/cm for Al-gate, 2.35 MV/cm for W-gate to 2.8 MV/cm for Au and TiN-gate) and goes to Pool-Frenkel for medium fields. For positive bias, fast increase of the current is observed over 2-3 V (1.2-1.75 MV/cm) which is due to the breakdown of the ultrathin SiO_2 at the interface with Si. The conduction mechanism for this region is combination of Fowler-Nordheim tunneling (FN) through SiO_2

and PF through Ta_2O_5 (Pecovska-Gjorgjevich et al., 2004).

Figure 2 shows high frequency *C-V* characteristics of structures with different gate electrodes at 1MHz. The measured value of accumulation capacity was 5.5 μF/cm^2 for Au, 5.14 μF/cm^2 for Al, 4.56 μF/cm^2 for W and 5.02 μF/cm^2 for TiN as a gate. The difference in capacitance values for different MOS structures come from different work functions of gate electrode and the concentration of defects on the interface between the gate and the oxide, generated during the deposition process. In order to discuss their influence on the capacitance value and leakage currents, the work functions of the gate materials were used from the literature, Au (Φ = 5.1eV), Al (Φ = 4.26eV), W (Φ = 4.55eV) and TiN (Φ = 4.95eV) (Wyon, 2002). Larger work function of Au results in higher values of capacitance and lower leakage currents confirming good contact between Au and oxide without high concentration of interface defects. The lowest value of capacitance for W is connected to lowest value of its work function. Al on the other hand have higher values of capacitance, similar to TiN gate structures and higher leakage current

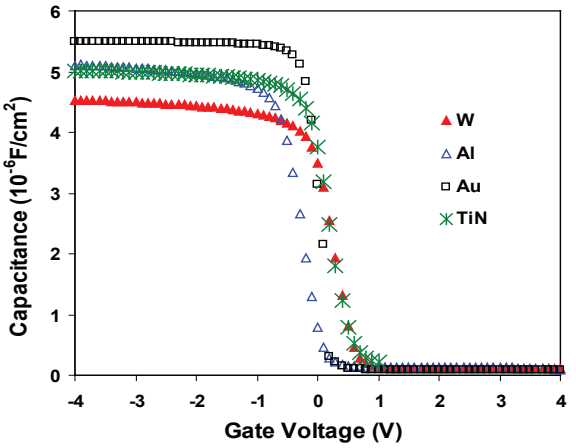

Figure 2 High-frequency *C-V* curves for rf sputtered oxides with different gate electrodes

although his work function is lower than tungsten's or TiN. The explanation could be in the reaction of Al with Ta_2O_5 and high generation of traps at the interface of gate and the oxide (Atanassova et al., 2008). The relative dielectric constant of the structures including the interfacial SiO_2 layer was estimated to 10.8, 9.9, 8.6 and 9.7 respectively.

Breakdown field E_{BD} was measured for all films and it was taken to be the highest value of the voltage during the stress. The characteristic time-dependent voltage curve for Ta_2O_5 does not show catastrophic breakdown like the one for SiO_2, but so called soft breakdown. The initial stage of time dependence of the gate voltage shows increase of the external field connected to negative charge trapping referring to the presence of pre-existing electron traps in the oxide. After the maximum of the voltage is reached, these oxide films exhibit an additional slow decrease for a long time afterwards, which is happening because of the slow degradation of the SiO_2 interfacial layer. In this stage the slow positive charge build-up takes place and negative charge is releasing (Roderick, 1980). Similar curves are obtained for Au, Al and W gate electrode. TiN gate MOS structures show different behavior depending on injected current.

Breakdown field for tungsten gate structures is estimated around 3.25 MV/cm, ~6 MV/cm for gold electrode, and over 6 MV/cm is measured for aluminum gate MOS structures. Higher injected currents through the oxide initiate higher values of breakdown voltage.

Figure 3 shows time-dependent curve of voltage during constant current stress (CCS) with current density J = - 0.02 A/cm^2, - 0.2 A/cm^2 and - 4 A/cm^2 for Au gate MOS structures. Observing the initial part of curves, we can see that the value of the injected current does not affect the behavior of the structure. The initial voltage is approximately

same for all injected currents (2.5-2.8V), suggesting the low concentration of defects in the interlayer Au-Ta_2O_5. Maximum value is reached for very short time, i.e. for very small amount of charge injected (1C/cm^2 for 0.02A/cm^2), followed by slow degradation during further injection of constant current. Higher current density initiates higher electric field across the structure (faster generation of interface positive charges appears), probably because of the presence of hydrogen in the interface because of post metallization annealing in H_2.

The stability of the dielectric was observed by sweeping the voltage from inversion to accumulation and back in interval (5V to -5V and back to 5V). Hysteresis in C-V curves is usually connected to charge trapping in the states near the interface with Si. Figure 4 shows negative hysteresis behavior of the *C-V* curve, which indicates the presence of interfacial traps in the oxide defect states, when the structure is under stress. The sign of these interfacial traps appears to be positive which is obtained from the negative voltage shift in the high frequency *C-V* characteristics, due to the presence of slow states at Si/SiO_2 interface (Dimitrova et al., 2001). The negative shift is observed for all investigated structures. Small hysteresis effect in Au gate structures (0.1V) suggests small density of slow border states. The biggest shift is observed for Al gate structures, 0.8V, while W gate and TiN gate structure exhibit similar values 0.45V and 0.4V respectively.

The flat band voltage V_{FB} can be directly obtained from the experimental dependence $1/C^2$ *vs* V_g curve as intercept with the V_g axis. The result of V_{FB} for Au gate MOS structures is given in Figure 5. This gives us information about the value of the work function Φ_{ms}, ($V_{FB} = \Phi_{ms} = \Phi_m - \Phi_s$), as well as the doping concentration N_A (Di Maria et al., 1993; Sze, 2001). The obtained flat band voltage V_{FB} for Ta_2O_5-SiO_2-Si structures with different gates were: 0.1V for Au gate, 0.4V for structures with W as a gate, -0.2V for Al gate, and 0.2V for TiN gate. The results from Figure 4 and Figure 5 indicate the acceptors as generated traps. The number of the slow trapping states, N_A is estimated using the equation $N_A = C\Delta V_{fb}/(eS)$, (Lai et al., 2002) where C is the capacitance of the oxide, ΔV_{fb} is the hysteresis loop of the flat band voltage, e is the electron charge and S is the capacitor area. The extracted values of N_A for structures

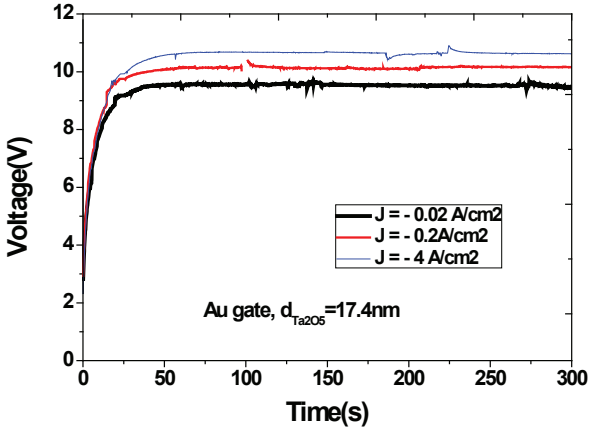

Figure 3 Voltage *vs* time during CCS for Au-Ta_2O_5-SiO_2-Si structures with three different injected currents from the gate

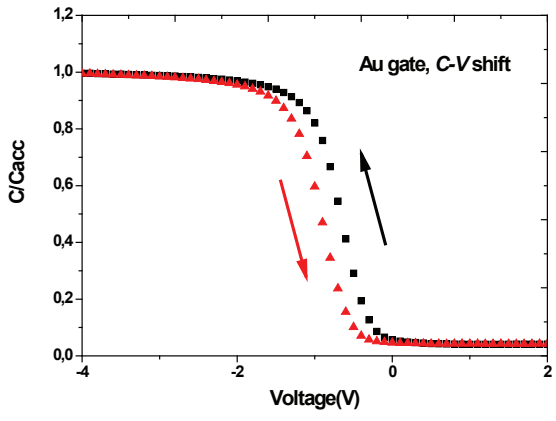

Figure 4 The hysteresis effect in MOS structures with Au gate electrode. First curve gives changes from inversion to accumulation, the second opposite direction.

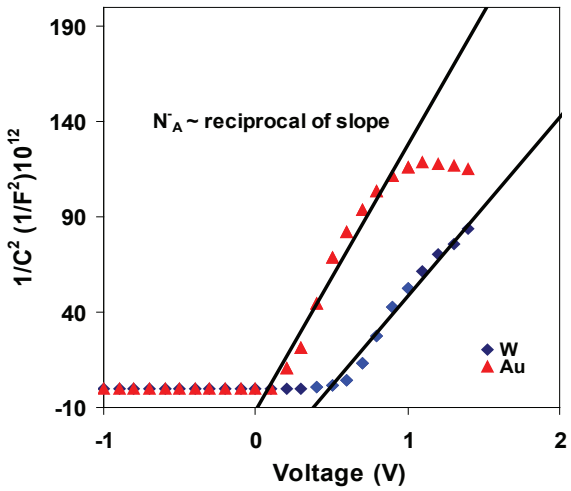

Figure 5 $1/C^2$ *vs* V_g for Au and W-gate MOS structure

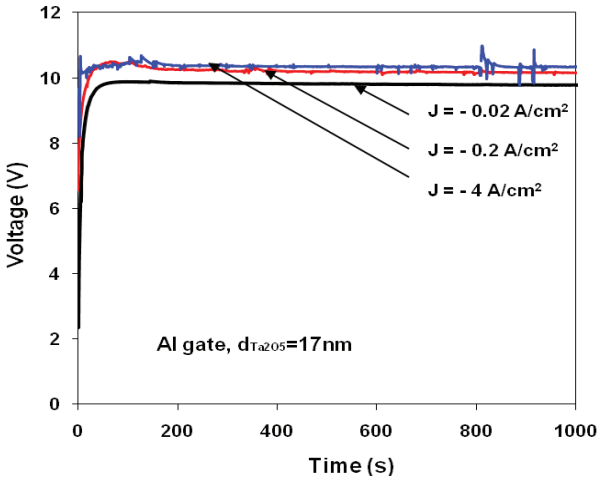

Figure 6 Long term *V-t* curves for Al gate oxides for three different injected currents

with Au, Al, W and TiN gate were $1.6x10^{11}cm^2$, $3,3x10^{12}cm^2$, $1.33x10^{12}cm^2$ and $7.8x10^{11}cm^2$ respectively.

Since the Ta_2O_5 layers of all four MOS structures were deposited with the same process, the difference in their electrical properties comes from the interaction between the gate material and Ta_2O_5 and the generation of interfacial positive traps. Seems that Al gate structures present more positive charges which may be attributed to the deposition method of evaporation, while structures with Au as a gate have lowest value of these traps, suggesting good compatibility between Au and Ta_2O_5.

The evolution of the *V-t* curves during constant current stress for Al-gate MOS structures for three current densities injected from the gate, – 0.02 A/cm², – 0.2 A/cm² and – 4 A/cm² is given in Figure 6. The initial behavior of these structures is different from what we observed for Au-gate capacitors. The initial voltage for injected current of –0.02 A/cm² is 2.35 V, 6.56 V for -0.2 A/cm² and 9.58 V for -4 A/cm² injected current density. The higher injected current initiates the higher initial voltage suggesting the presence of native positive traps and lots of defects in the interfacial layer between Al and Ta_2O_5. The initial dropping of the voltage before increasing due to existence of the positive charge traps in the structures characteristic for thicker films not submitted to H_2 post metallization annealing (Novkovski et al., 1999; Pecovska-Gjorgjevich et al., 2004) is not observed in our thin films.

The charge trapping behavior of the samples with Au and Al gate, observed by continuously monitoring of the change in gate voltage ($\Delta V_g = V_g - V_{g0}$, V_{g0} is the initial value of the voltage on the structure), required to maintain a constant current of different values under gate injection is shown in Figure 7 for Au and Figure 8 for Al gate. The difference in those two types of structures is obvious; while Au-gate structures have higher ΔV_g with higher injected currents, the Al-gate structures show opposite behavior, the higher injected current, the lower voltage change. This confirms the absence of defects in the first structure and their proportional creating with increasing the injected current.

The initial fast increase of the voltage for Al gate MOS structures, more pronounced for lower stressing currents is due to the filling of native

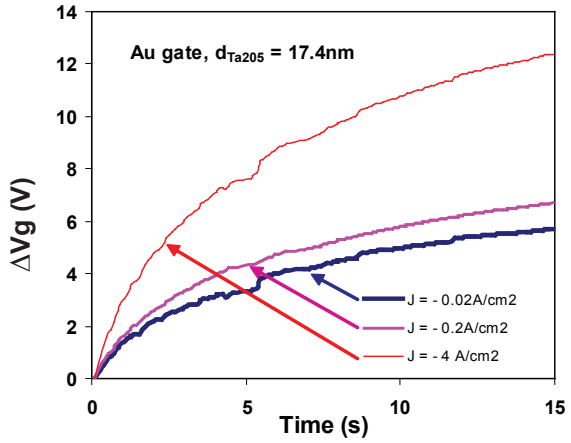

Figure 7 ΔV_g *vs* time in the initial moments of stress for Au gate electrode capacitors and different injected currents

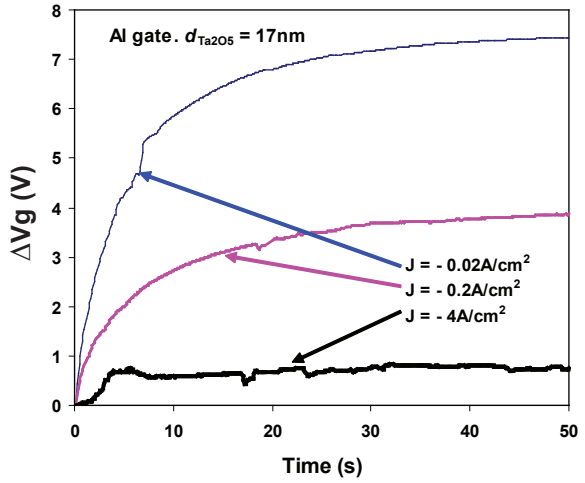

Figure 8 ΔV_g *vs* time in the initial moments of stress for Al gate electrode capacitors and different injected currents.

traps and high rate of generation of new traps, with enough time for slow positive traps to be created, unlike very low increasing rate of the voltage for higher injecting currents. The increasing of the voltage-time curve happens in the initial 50-100 s. Afterward we observe very slow degradation of the film, i.e. impact ionization of neutral traps leading to release of the electrons or positive charge built -up. This is mutual for all investigated structures and is characteristic behavior for Ta_2O_5 structures.

Oxide structures with W gate electrode show no difference in the curve depending on low and high currents injected. They have very similar behavior like Au-gate structures. The negative *C-V* shift and sharp voltage rate in short time (30s) with low injected charge (6C/cm^2 for 0.2A/cm^2), confirms the existence of imperfections at Si/SiO_2 interface. A presence of high concentration of traps at the W-oxide interface (radiation defects generated during the sputtering of W) (Atanassova et al., 2008) is the reason for high initial voltage for all structures and all injected currents. The space charge in the oxide affects the barrier height which affects the gate voltage (Nandi et al., 2003). The initial change in gate voltage (ΔV_g) during first 50s, under gate injection for W is shown in Figure 9. The slow degradation without catastrophic breakdown in the late stage is similar with the other films and is refer as soft breakdown.

MOS structures with d =17 nm and with TiN electrode on the top represented bad voltage/time characteristics during stress period with very low current injected (0.001 A/cm^2), suggesting that the reactive sputtering is maybe not suitable method for obtaining capacitors with this gate material, or they can be used for very low injected currents. Instead, the films with thickness of 34 nm and TiN as gate material are submitted to CCS with different current density, Figure 10. Low injected current initiates very low change of the voltage, i.e. low concentration of pre-traps exist in the structures (which is confirmed with low leakage currents results), but the second stage of catching positive charge is more pronounced till 50s. The higher injected currents lead to massive catch of electrons in the initial stage, suggesting that the rate of creation of negative charge traps during injection from the gate is high.

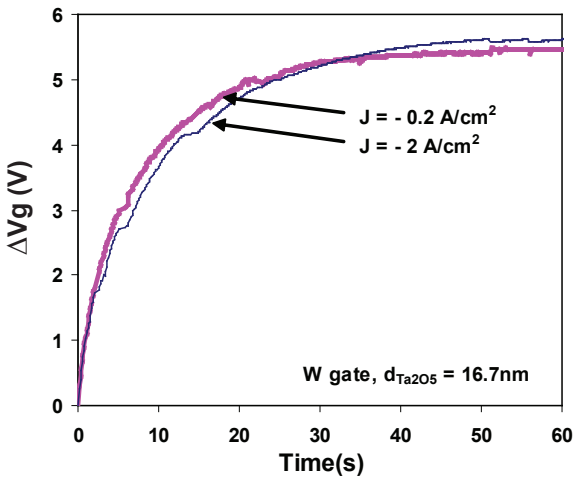

Figure 9 ΔV_g *vs* time for structures with W as a gate electrode in the initial moments of stress

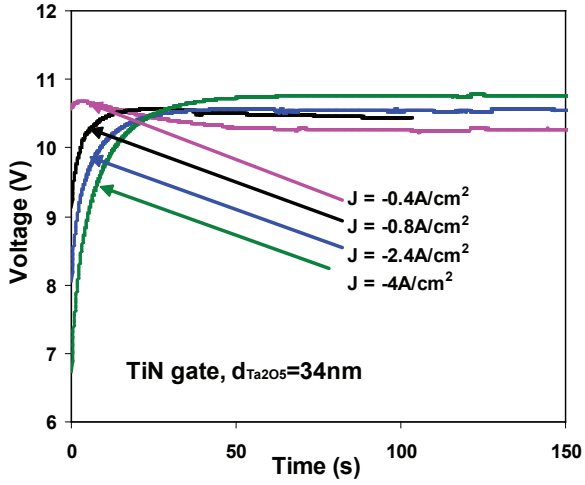

Figure 10 Voltage *vs* time during constant current stress for TiN gate with thicker Ta_2O_5 layer.

Conclusion

Electrical characteristics of MOS structures of Ta_2O_5–SiO_2–Si with different gate electrodes (Al, Au, W, TiN) are investigated. The results show high capacitance density and low leakage currents (below 10^{-7}A/cm² for ±1V) for Au-gate structures which put them in the group of materials for possible application in DRAM industry. *C-V* shift confirms presence of traps in the structures generated during deposition process of the gate, lowest for Au and highest for Al.

The structures are also submitted to constant current stress with various current densities. The evolution of the obtained curves shows fast increase in the beginning (due to the filling of native traps and a high rate of generation of new traps) followed by a slow evolution, mainly caused by the reduction of generation rate due to trapping. The time-dependent voltage curves reveal difference between various gate oxides in the initial stage. The presence of the pre-existing traps in the interface gate electrode-oxide is responsible for the trapping kinetics common for all structures, but with differences in the initial behavior.

Different initial voltage over the structure observed for different injected currents densities of Al gate MOS capacitors implies for lower rate of creating new traps during stress with higher currents. This effect is not observed for Au and W gate structures, where we see similar behavior of the structures under different CCS. Increasing the voltage through the structure with increasing the injected constant current is observed for Au-gate structures. Lower initial voltage for Au structures show lower concentration of traps generated during deposition process than Al-gate structures connected to the reaction between Al and the oxide. The change of the voltage during different CCS is almost the same for W-gate structures, indicating that the defect concentration in the oxide and interface oxide-gate generated during deposition process is much higher than concentration of the charge traps generated during CCS.

The second stage of voltage-time curves is characterized with positive charge build-up and new bulk traps generation for all films, expressing with slow degradation. This behavior is relatively same for all the films.

TiN-gate MOS structures with thinner oxide layer degrade very fast, so we observed thicker (34nm) films which pronounced different behavior in the initial stage.

From all the structures investigated we can distinguish the one with Au gate. This structure has low leakage current density and from the high breakdown conditions, as well as from the high values of the accumulation capacity, it reaches the required demands for its application in microelectronic industry. The CCS measurements show these structures as reliable in long term. As we know, gold is an excellent conductor, so it is not surprise to see that it has the lowest current density and high accumulation capacity (Nandi et al., 2003; Atanassova et al., 2008). This material could be considered as promising candidate for such structures in future MOS technology.

References

Atanassova, E., Novkovski, N., Paskaleva, A., and Pecovska-Gjorgjevich, M. (2002) Oxygen annealing modification of conduction mechanism in thin rf sputtered Ta_2O_5 on Si. *Solid State Electronics* 46: 1887-1898.

Atanassova, E. and Paskaleva, A. (2007) Challenges of Ta_2O_5 as high-k dielectric for nanoscale DRAMs. *Microelectronics Reliability* 47 (6): 913-923.

Atanassova, E. and Spassov, D. (2000) Thin Ta_2O_5 Films on Si by XPS. *Surface Science Spectra* 7: 143.

Atanassova, E., Spassov, D., Paskaleva, A., Koprinarova, J., and Georgieva, M. (2002) Influence of oxidation temperature on the microstructure and electrical properties of Ta_2O_5 on Si. *Microelectronics Journal* 33: 907-920.

Atanassova, E. and Spassov, D. (1999) Hydrogen annealing effects on the properties of thermal Ta_2O_5 on Si. *Microelectronics Journal* 30: 265-274.

Atanassova, E., Dimitrova, T., and Koprinarova, J. (1995) AES and XPS study of thin RF-sputtered Ta_2O_5 layers. *Applied Surface Science* 84: 193-202.

Atanassova, E., Paskaleva, A., and Novkovski, N. (2008) Effects of the metal gate on the stress-indusced traps in Ta_2O_5/SiO_2 stacks. *Microelectronics Reliability* 48: 514-525.

Atanassova, E., Stojadinovic, N., Paskaleva, A., Spassov, D., Vracar, L., and Georgieva, M. (2008) Constant voltage stress induced current in Ta_2O_5 stacks and its dependence on a gate electrode. *Semiconductor Science Technologies* 23: 075017.

Brown, G. A. (2004) Scaling CMOS Materials & devices. *Materials Today* 7(1): 20-25.

Di Maria, D. J., Cartier, E., and Arnold, D. (1993) Impact ionization, trap creation, degradation, and breakdown in silicon dioxide films on silicon. *Journal of Applied Physics* 73: 3367-3384.

Dimitrova, T., Arshak, K., and Atanassova, E. **(**2001) Crystallization effects in oxygen annealed Ta_2O_5 thin films on Si, *Thin Solid Films* 381: 31-38.

Gilmer, D., Hobbs, C., Hegde, R., La, L., Adetutu, O., Conner, J., Tiner, M., Prabhu, L., Bagchi, S., and Tobin, P. (2000) Investigation of titanium nitride gates for tantalum pentoxide and titanium dioxide dielectrics. *Journal of Vacancy Science and Technology A* 18, 1158.

Groner, M. D. and George, S. M. (2003) High-k dielectrics grown by atomic layer deposition : Capacitor and gate applications. In *Interlayer Dielectrics for Semiconductor Technologies,* **(**Murarka I., Eizenberg S. P., and Sinha, A.

K., eds.), pp. 327-348. Academic Press, San Diego.

International Technology Roadmap for Semiconductors (ITRS), [Online URL: www.http://public.itrs.net].

Jiang, P. C. and Chen, J. S. (2004) Effects of Post-Metal Annealing on Electrical Characteristics and Thermal Stability of W_2N/Ta_2O_5 /Si MOS Capacitors. *Journal of The Electrochemical Society* 151(11): 751-755.

Kingon, A., Maria, J., and Streiffer, S. (2000). Alternative dielectrics to silicon dioxide for memory and logic devices. *Nature* 406: 1032-1038.

Lai, Y., Chen, K., and Chena, J. S. (2002) Investigation of the interlayer characteristics of Ta_2O_5 thin films deposited on bare, N_2O, and NH_3 plasma nitridated Si substrates. *Journal of Applied Physics* 91(10): 6428-6434.

Lee, B. H., Choi, R., Kang, L., Gopalan, S., Nieh, R., Onishi, K., Jeon, Y., Qi, W.- J., Kang, C., and Lee, J. C. (2000) Morphology and crystallization kinetics in HfO2 thin films grown by atomic layer deposition. *Tech. Dig. - International Electron Devices Meeting,* 39.

Lee, J. W., Han., C. H., Park, J. -S., and Park, J. W. (2001) Dry etching of ZnO thin film by Inductively Coupled plasma. *Journal of Electrochemical Society* 148: 95.

Nalwa, H. S., Ed. (1999). *Handbook of Low and High Dielectric Constant Materials and Their Applications, Volume 1: Materials and Processing*. Academic Press, San Diego.

Nandi, S. K., Chatterjee, S., Samanta, S. K., Dalapati, G. K., Bose, P. K., Varma, S., Patil, S., and Maiti, C. K. (2003) Electrical properties of Ta_2O_5 films deposited on ZnO. *Bulletin of Materials Sciences* 26(4): 365-369.

Nishioka, Y., Kimura, S'i., Shinriki, H., and Mukai, K. (1987) NMR spectrum of 4 contained six resonances for the epoxy carbon. *Journal of Electrochemical Society* 134: 410.

Novkovski, N., Pecovska-Gjorgjevich, M., Atanassova, E., and Dimitrova, T. (1999) Stress degradation of low field leakage in aluminium gate MOS structures containing RF magnetron sputtered thin Ta_2O_5 films on silicon. *Physica Status Solidi* (a) 172: R9-R10.

Novkovski, N. and Atanassova, E. (2005) Wearout and breakdown of RF Sputtered Ta_2O_5 Films on Silicon. *Applied Physics A* 81(6): 1191-1195.

Pecovska-Gjorgjevich, M., Novkovski, N., and Atanassova, E. (2003) Stress induced leakage currents in thin Ta_2O_5 films. *Microelectronics Reliability* 47: 235-241.

Pecovska-Gjorgjevich, M., Novkovski, N., Atanasova, E., and Spassov, D. (2004) The effect of gate material on dielectric characteristics and conduction of Ta_2O_5 MOS structures. *Proceedings of the 2004 IEEE International Conference on Solid Dielectrics ICSD* 872-875.

Pecovska-Gjorgjevich, M., Spassov, D., Novkovski, N., and Atanasova, E. (2005) Dielectric characteristics and reliability tests for thin Au-Ta_2O_5-SiO_2-Si structures. *Romanian Journal of Physics* 50: 1009-1017.

Roderick, E. H. (1980) Metal-Semiconductor Contacts. In *Monograph in Electrical and Electronic Engineering* (Hammand, P. and Walsh, D., eds.), p.10. Oxford University Press, England.

Spassov, D., Atanassova, E., and Virovska, D. (2006) Electrical characteristics of Ta_2O_5 based capacitors with different gate electrodes. *Applied Physics A: Materials Science & Processing* 82: 55-62.

Sze, S. M. (2001) *Physics of Semiconductor Devices*, John Wiley & Sons, New York.

Swartz, S. L. (1990) Topics in electronic ceramics. *IEEE Transactions on Electrical Insulation* 25: 935-987.

Vehkamaki, M., Hanninen, T., Ritala, M., Leskela, M., Sajavaara, T., Rauhala, E., and Keinonen, J. (2001) Atomic layer deposition of SrTiO3 thin films from a novel strontium precursor - strontiumbis(tri-isopropylcyclopentadienyl). *Chemical Vapor Deposition* 7: 75-80.

Wilk, G. D., Wallace, R. M., and Anthony, J. M. (2001) High-κ gate dielectrics: Current status and materials properties considerations. *Journal of Applied Physics* 89(10): 5243-5276.

Wyon, C. (2002) Future technology for advanced MOS devices. *Nuclear Instrumentation and Methods in Physical Research* B 186: 380-391.