VDTA-Based Floating FDNR Simulator Topology

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Abstract

An electronically tunable floating frequency-dependent negative resistance (FDNR) simulator circuit is presented in this paper. The circuit is composed of only three voltage differencing transconductance amplifiers (VDTAs) and two grounded capacitors without any external resistors. The presented FDNR simulator can be tuned electronically by changing the transconductance value of the VDTA. As application examples, the fourth-order Butterworth bandpass and lowpass filters are simulated using the proposed tunable floating FDNR simulator. Finally, the simulation results using CMOS 0.35 μm TSMC process parameters are included to verify the theoretical analysis.

Keywords: Voltage Differencing Transconductance Amplifier (VDTA); Frequency-Dependent Negative Resistance (FDNR), Floating Simulator

1. Introduction

Frequency-Dependent Negative Resistances (FDNRs) are very useful elements for the design and synthesis active filter. Also, FDNR can be used in applications of using floating inductance [1]. Several FDNR implementations using various active devices were proposed in literature [2]-[9]. However, the works in [2]-[8] require at least three passive components and most of them are floating. In [9], at least four active components were realized. Recently, the newly versatile active building block, namely voltage differencing transconductance amplifier (VDTA), has been introduced [10]. This element is composed of the current source controlled by the difference of two input voltages and a multiple-output transconductance amplifier, providing electronic tuning ability through its transconductance gains. This means that the VDTA device is very suitable for electronically tunable active circuit synthesis. Another advantageous feature of the use of the VDTA as an active element is that compact structures in some applications can be achieved easily [11].

In this paper, the proposed approach of the floating FDNR simulator topology is studied. The realized FDNR consists of three VDTAs and two grounded capacitors; accordingly, it is suitable for integrated circuit (IC) implementation point of view. The value of the simulated FDNR is electronically tunable by adjusting the bias current of the VDTA. The performance of the proposed tunable FDNR is demonstrated on example of fourth-order Butterworth filter design. Computer simulations are given to confirm the theory and to show the performance of the circuits.

2. Basic Concept of The VDTA

As symbolically shown in Fig.1, the VDTA device is an active five-terminal building block, when p and n are input terminals, and z, +x and -x are output terminals. The terminal relations of this device can be expressed by the following matrix equation [10]-[11] :

$$\begin{bmatrix} i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} g_{mF} & -g_{mF} & 0 \\ 0 & 0 & g_{mS} \\ 0 & 0 & -g_{mS} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \quad (1)$$

where g_{mF} and g_{mS} are the first and second transconductance gains of the VDTA, respectively. From eq.(1), the differential input voltage from p and n terminals (v_p–v_n) is transformed into the current through the terminal z (i_z) by the transconductance g_{mF}. The voltage drop at the terminal z (v_z) is then converted to output currents at the terminals +x (i_{x+}) and -x (i_{x-}) by the transconductance g_{mS}. In general, the transconductance gains of the VDTA can be controlled electronically by the external bias voltage/current.

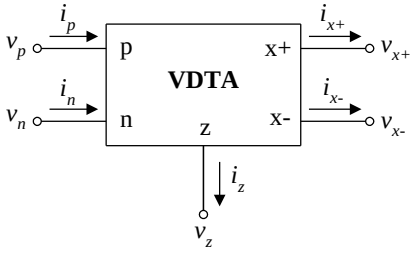

Figure 1. Circuit symbol of the VDTA.

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Recently, the simple CMOS realization of the VDTA is introduced in [11]. Fig.2 shows the internal structure of the circuit, which is composed of two Arbel-Goldminz transconductances [12]. In this case, the g_{mF}- and g_{mS}–values of this element are determined by the output transistor transconductance, which can respectively be approximated as :

$$g_{mF} \cong \left(\frac{g_1 g_2}{g_1 + g_2}\right) + \left(\frac{g_3 g_4}{g_3 + g_4}\right) \tag{2}$$

and

$$g_{mS} \cong \left(\frac{g_5 g_6}{g_5 + g_6}\right) + \left(\frac{g_7 g_8}{g_7 + g_8}\right) \tag{3}$$

where $g_i = \sqrt{I_{Bi}\mu C_{ox}\frac{W_i}{L_i}}$

Here g_i is the transconductance value of the i-th transistor (i = 1, 2, …, 8), I_{Bi} is the bias current of the i-th transistor, μ is the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the effective channel width and length of the i-th MOS transistor, respectively.

3. Proposed Floating FDNR Circuit

Fig.3 shows the proposed floating FDNR simulator circuit. This realization employs three VDTAs and two grounded that is attractive from the fabrication point of view. It can be derived that the admittance matrix for the configuration of Fig.3 is given by :

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{s^2 C_1 C_2 g_{m1}}{g_{mF2} g_{m3}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{4}$$

where $g_{m1} = g_{mF1} g_{mS1}$ and $g_{m3} = g_{mF3} g_{mS3}$. Thus, the circuit of Fig.3 realizes a floating FDNR with an equivalent floating admittance given by :

$$Y_{eq} = s^2 D_{eq} = \frac{s^2 C_1 C_2 g_{m1}}{g_{mF2} g_{m3}} \tag{5}$$

where $D_{eq} = \frac{C_1 C_2 g_{m1}}{g_{mF2} g_{m3}}$.

From eq.(5), it is easy to see that the value of the FDNR can be tuned by electronic means through either g_{mF} or g_{mS} of the VDTA. In addition, if we let $V_1 = 0$ or $V_2 = 0$, then the tunable grounded FDNR can easily be realized.

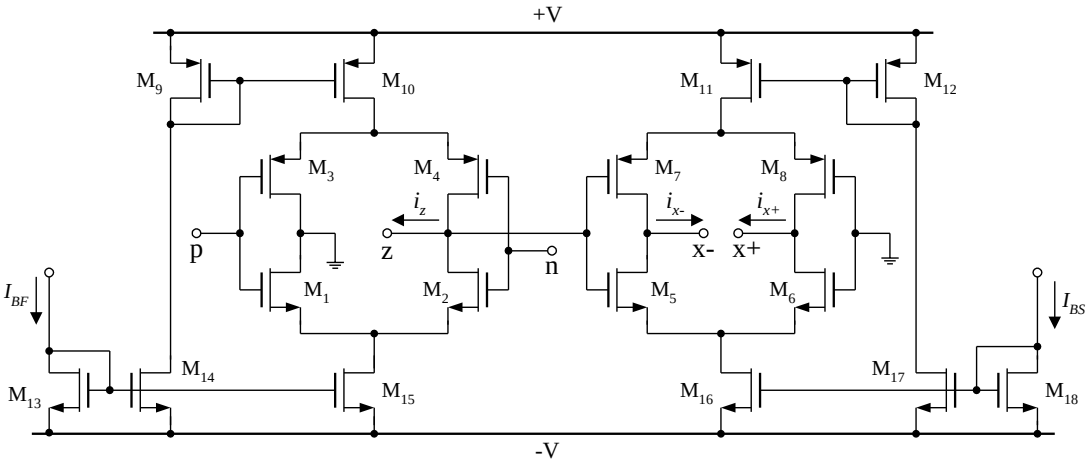

Figure 2. CMOS implementation of the VDTA.

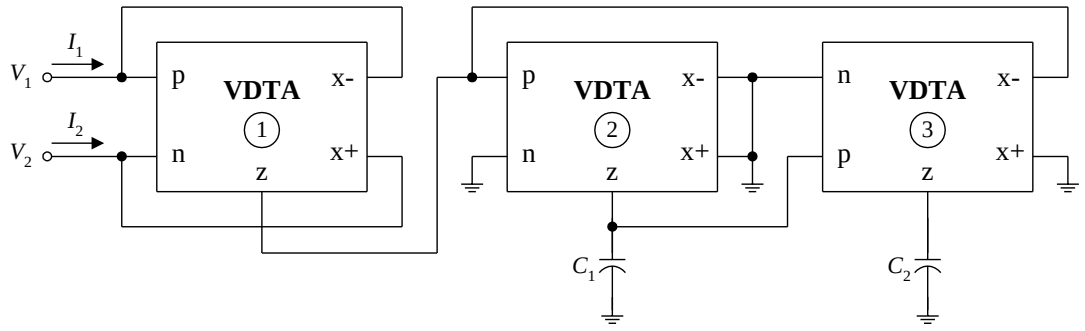

Figure 3. Proposed floating FDNR simulator using VDTAs.

4. Performance Verification by Computer Simulation

In order to evaluate the behavior of the proposed circuit in Fig.3, it is simulated using PSPICE simulation. In simulations, the VDTA was performed by the schematic CMOS implementation given in Fig.2 with supply voltages +V = -V= 1.8 V. The CMOS transistors in VDTA implementation were simulated the 0.35 μm TSMC process parameters. The dimensions of MOS transistors are given in Table I.

TABLE I. Dimensions of MOS transistors in Fig.2.

Transistors	W (μm)	L (μm)
$M_1 - M_2$, $M_5 - M_6$	16.1	0.7
$M_3 - M_4$, $M_7 - M_8$	28	0.7
$M_9 - M_{12}$, $M_{14} - M_{17}$	56	0.7
M_{13} , M_{18}	7	0.7

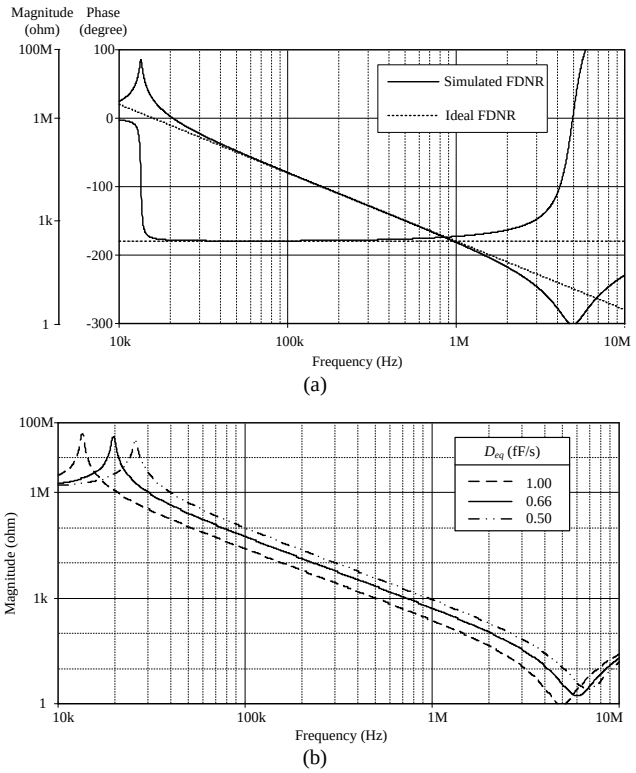

Figure 4. Frequency responses of impedance of the proposed tunable floating FDNR simulator circuit in Fig.3. (a) magnitude and phase characteristics (b) electronic tuning of the D_{eq}-value.

As an example, the component values were chosen as : $C_1 = C_2 = 1$ nF, $g_{mF1} = g_{mS1} = g_{mF2} = g_{mS2} \cong 0.60$ mA/V ($I_{BF1} = I_{BS1} = I_{BF2} = I_{BS2} = 100$ μA), and $g_{mF3} = g_{mS3} \cong 0.77$ mA/V ($I_{BF3} = I_{BS3} = 200$ μA), which results in $D_{eq} = 1$ fFs. Fig.4(a) shows the frequency response of the impedance of the proposed floating FDNR simulator circuit in Fig.3 relative to frequency. It can be observed that the circuit operates pretty well between 20 kHz and 2 MHz. To further demonstrate the electronic tunability of the proposed FDNR, the simulator was also simulated by varying g_{mF3} ($= g_{mS3}$) $\cong 0.77$ mA/V, 0.93 mA/V and 1 mA/V, to obtain $D_{eq} = 1.00$ fFs, 0.66 fFs, and 0.50 fFs, respectively. The frequency characteristics of the inductance simulator for various g_{mF3} values are shown in Fig.4(b). As depicted in Fig.4, the simulation results are in close agreement with the prediction, and confirm that the value of D_{eq} can be adjusted electronically by the transconductance gain of the VDTA.

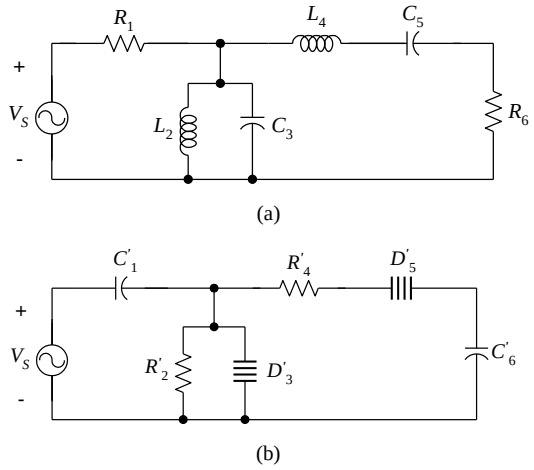

Figure 5. Fourth-order Butterworth bandpass filter. (a) RLC passive prototype (b) equivalent CDR circuit with FDNRs.

5. Application Examples

In this section, the proposed floating FDNR simulator in Fig.3 is used in the RLC fourth-order Butterworth bandpass filter prototype shown in Fig.5(a), where $R_1 = R_6 = 1$ Ω, $L_2 = 0.225$ μH, $C_3 = 1.225$ μF, $L_4 = 11.25$ μH, $C_5 = 22.5$ nF [13]. This filter is designed to obtain fourth-order Butterworth characteristic whose bandwidth and center frequency are $BW = 32$ kHz and $f_o = 316$ kHz respectively. By applying Bruton transformation [14] and using magnitude scaling constant ($k_m = 10^9$) and variable impedance scaling method, i.e. dividing the impedance of each element in the Fig.5(a) by k_m, the RLC passive filter is converted into CRD filter as shown in Fig.5(b) where all FDNRs are realized using the proposed circuit in Fig.3. In Fig.5(b), the resulting circuit components are obtained as : $C'_1 = 1$ nF, $R'_2 = 225$ Ω, $D'_3 = 11.25$ fFs, $R'_4 = 11.25$ kΩ, $D'_5 = 11.25$ aFs, and $C'_6 = 1$ nF. According to these

component values, the voltage transfer function of the bandpass filter in Fig.5(b) is given by :

$$H(s) = \frac{(4.043 \times 10^{10})s^2}{s^4 + (2.843 \times 10^5)s^3 + (7.925 \times 10^{12})s^2 + (1.121 \times 10^{18})s + (1.554 \times 10^{25})} \quad (6)$$

The magnitude and phase characteristics of the filters are shown in Figs.6(a) and 6(b), respectively. From the figures, it appears that the theoretical and simulated results are in good agreement.

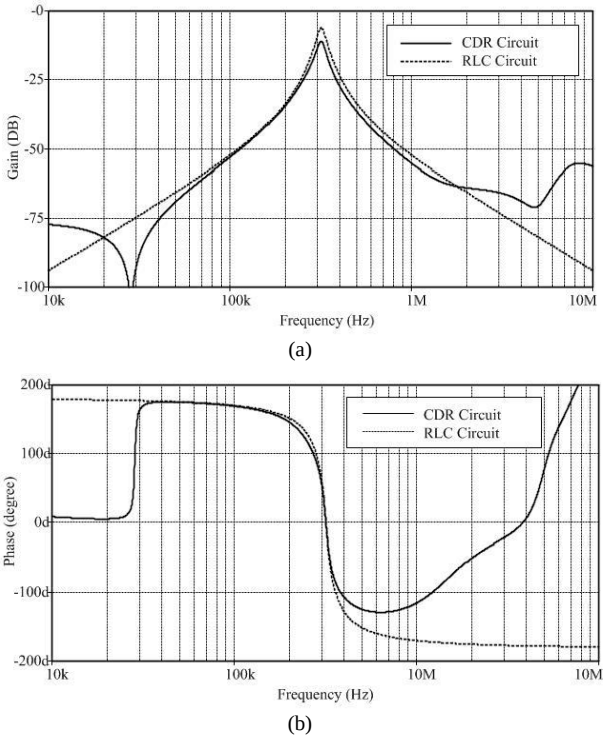

Figure 6. Simulated frequency characteristic of the filter in Fig.5. (a) gain response (b) phase response.

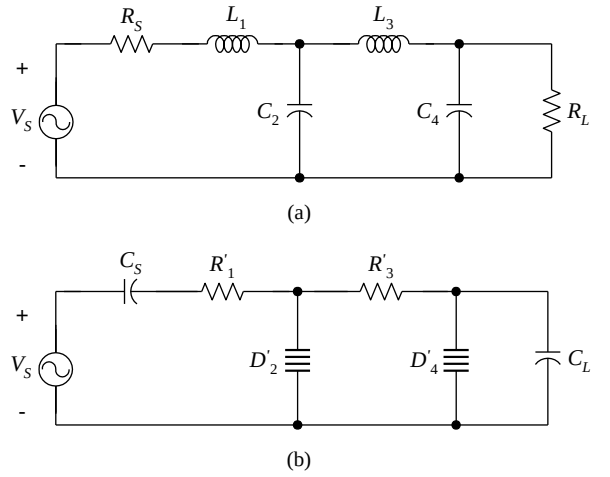

Figure 7. Fourth-order Butterworth lowpass filter. (a) RLC passive prototype (b) equivalent CDR circuit with FDNRs.

To illustrate another application of the proposed FDNR simulator, a fourth-order Butterworth lowpass filter shown in Fig.7(a) was designed and simulated. In Fig.7(a), the normalized component values are $R_S = R_L = 1\ \Omega$, $L_1 = 0.7654$ H, $C_2 = 1.848$ F, $L_3 = 1.848$ H and $C_4 = 0.7654$ F [15]. By applying Bruton transformation [14] and selecting $k_m = 1.59 \times 10^3$ and frequency scaling constant $k_f = 628.32 \times 10^3$, the prototype RLC passive filter in Fig.7(a) can be transformed to the CRD filter as shown in Fig.7(b) where the elements D'_2 and D'_4 were constructed using the proposed simulator circuit in Fig.3. As a result, the de-normalized component values of Fig.7(b) were obtained as : $C_S = C_L = 1$ nF, $R'_1 = 1.22$ kΩ, $D'_2 = 2.94$ fFs, $R'_3 = 2.94$ kΩ and $D'_4 = 1.22$ fFs. The simulated gain and phase characteristics of the fourth-order Butterworth lowpass filters in Fig.7 are displayed in Figs.8(a) and 8(b), respectively.

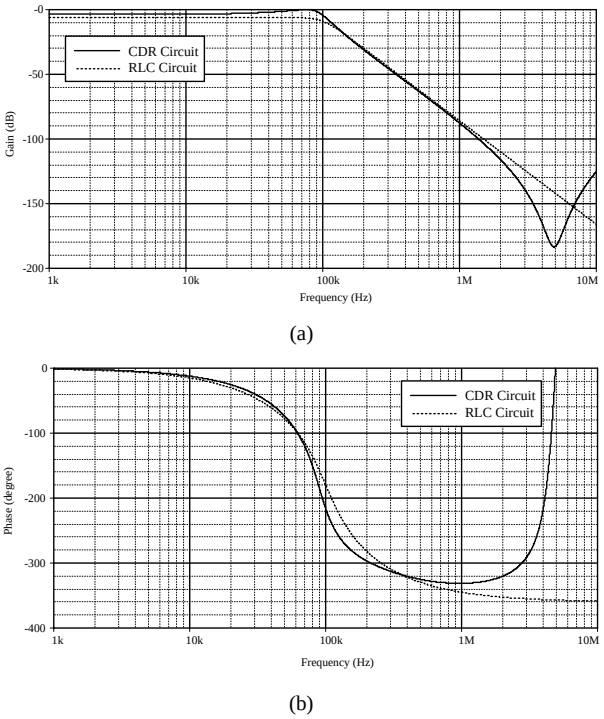

Figure 8. Simulated frequency characteristics of the filters in Fig.7. (a) gain response (b) phase response.

6. Conclusion

This paper describes an electronically tunable floating FDNR simulator circuit based on the use of the voltage differencing transconductance amplifier (VDTA) and only two grounded capacitor. The important gain of floating FDNR simulator is that its value can be adjusted electronically by changing bias currents of the VDTAs. To demonstrate the performance of the proposed circuit, it is used to construct fourth-order Butterworth bandpass and lowpass filters. PSPICE simulation results verify that the performances of the proposed circuit and its applications are in good agreement with the prediction of the analysis performed.

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