Hardware Development of Baseband Transceiver and FPGA-Based Testbed in 8×8 and 2×2 MIMO-OFDM Systems

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ABSTRACT

Multiple-input multiple-output orthogonal frequency multiplexing (MIMO-OFDM) is powerful in enhancing communication capacity or reliance. The IEEE802.11n standard defines use of four spatial streams in spatial division multiplexing (SDM). The task group of IEEE802.11ac will extend it to eight spatial streams. We present an 8×8 MIMO-OFDM baseband transceiver compatible with the IEEE802.11ac specification. Two 8×8 MMSE MIMO detectors based on Streassen's matrix inversion have been designed for real-time MIMO detection. To demonstrate MIMO-OFDM transmission, we have prototyped a FPGA-based testbed in 2×2 MIMO-OFDM for field experiment and video transmission.

1. INTRODUCTION

Multiple-input multiple-output orthogonal frequency multiplexing (MIMO-OFDM) is powerful in enhancing communication capacity or reliance. MIMO-OFDM is currently adopted in IEEE802.11n WLAN systems [1]. In upcoming standardization of IEEE 802.11ac [2], use of eight spatial streams in single-user MIMO (SU-MIMO) is discussed. As MIMO spatial streams increase, computational and hardware complexities in MIMO-OFDM systems also greatly increase. It is a challenging to design a MIMO-OFDM transceiver with minimal hardware cost and power dissipation in VLSI implementation. Especially, MIMO detection needs high-speed computation due to its large computational cost. Hardware implementation of MIMO detection is one important issue. Related researches have tackled linear detectors in minimum mean squared error (MMSE) for 4×4 MIMO-OFDM systems in terms of a trade-off between computational complexity and detector performance [3], [4]. Our presented MMSE MIMO detectors use pipeline processing on a subcarrier basis and are superior in throughput performance [5], [6]. As the next step, we study hardware development of an 8×8 MIMO-OFDM transceiver compatible with the IEEE802.11ac specification.

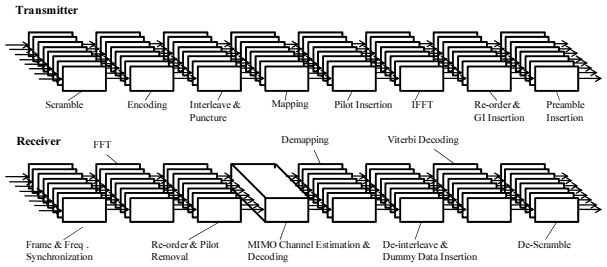

Fig.1: *Block diagram of 8×8 MIMO-OFDM transceiver.*

Since a 4×4 MIMO-OFDM baseband transceiver has been developed in our previous work [7], most part of circuit components can be re-used in the 8×8 MIMO-OFDM transceiver. An 8×8 MIMO detector requires a new design because of increasing matrix size and computational complexity by eight times as much as in 4×4 MIMO. We have designed two 8×8 MMSE MIMO detectors according to time variations in MIMO channels (i.e., fast and slow fading environments). The implementation result of the 8×8 MIMO-OFDM transceiver has been reported in circuit area and power dissipation.

We have prototyped a FPGA-based testbed in 2×2 MIMO-OFDM for field experiment and video transmission. Our testbed integrates baseband and RF units and can measure communication performance in bit error rate (BER) and packet error rate (PER). In the field experiment, we have evaluated outdoor MIMO characteristics in line-of-sight (LOS) and non-line-of-sight (NLOS) conditions. The video transmission equipment has extended the testbed by adding packet sending and receiving functions to deal with video streaming data.

This paper is organized as follows: In Section 2, we describe an 8×8 MIMO-OFDM baseband transceiver and its implementation. The FPGA-based testbed for field experiment and video transmission is reported in Section 3. Finally, Section 4 provides a conclusion.

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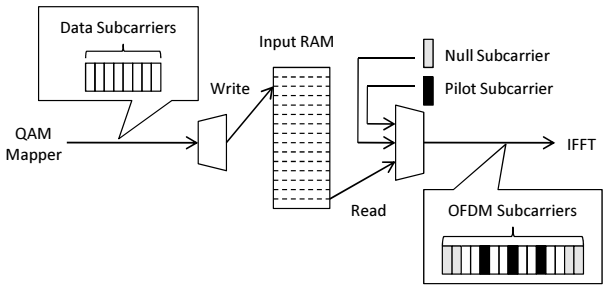

Fig.2: *Data buffering between QAM mapping and IFFT blocks.*

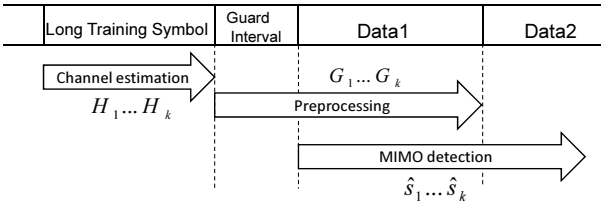

Fig.3: *Timing chart of MIMO detection.*

2. 8X8 MIMO-OFDM TRANSCEIVER

2.1 Block Diagram

A block diagram of an 8×8 MIMO-OFDM transceiver is shown in Fig. 1. The encoded data is mapped into QAM constellation points. OFDM modulated signals adding a cyclic prefix are transmitted by the eight outputs. The receiver performs synchronization, demodulation, and extraction of data and pilot subcarriers. Spatial decomposition is executed by MIMO channel estimation and MIMO detection. This requires considerable complexity, which causes difficulty in the VLSI implementation. A soft demapper computes a soft-bit metric including the signal to interference and noise ratio (SINR) for each space and frequency index. The soft-bit metric is inputted into the Viterbi decoder block. The PHY data is restored through de-scrambling in the last step. The maximum PHY data rate reaches 3 Gbps by use of an 80-MHz channel bandwidth. We previously investigated the frame formats of this channel in SISO-OFDM and 2×2 MIMO-OFDM systems in [8].

2.2 Data Buffering

Data buffering between QAM mapping and IFFT blocks is illustrated in Fig. 2. The null and pilot subcarriers are inserted into the data sequence of data subcarriers before IFFT operation. Note that the length of the data sequence is changed by inserting the null and pilot subcarriers. To maintain the same clock sampling rate, the input RAM is used as data buffering. Thus, embedded memory units are used to connenct the adjoined processing blocks in the transceiver.

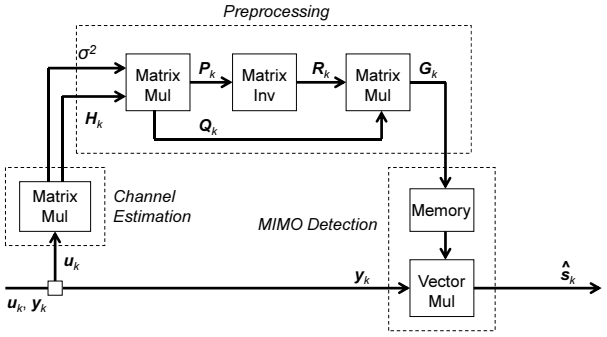

Fig.4: *Circuit structure of MIMO detector.*

2.3 MIMO Detection

MIMO-OFDM received signals $\boldsymbol{y}_k[t]$ with M_T transmitter and M_R receiver antennas are described by

$$\boldsymbol{y}_k[t] = \boldsymbol{H}_k \boldsymbol{s}_k[t] + \boldsymbol{n}_k[t], \tag{1}$$

where k is a subcarrier index, t is a data symbol index, $\boldsymbol{s}_k[t]$ is a signal transmitted at t-th symbol, and $\boldsymbol{n}_k[t]$ is a white Gaussian noise vector. $\boldsymbol{H}_k$ indicates a MIMO channel matrix whose elements are given the channel response from j-th transmitter antenna to i-th receiver antenna. The linear MIMO detection is classified into zero-forcing (ZF) and MMSE. The weight matrix $\boldsymbol{G}_k$ in the MMSE criterion is given by

$$\boldsymbol{G}_k = (\boldsymbol{H}_k^H \boldsymbol{H}_k + \sigma^2 \boldsymbol{I})^{-1} \boldsymbol{H}_k^H, \tag{2}$$

where $(\cdot)^H$ denotes the complex conjugate transpose, and σ^2 is the noise variance. The decoded signal $\hat{\boldsymbol{s}_k}[t]$ is decoded by multiplexing the weight matrix to the received signal as

$$\hat{\boldsymbol{s}_k}[t] = \boldsymbol{G}_k \boldsymbol{y}_k[t]. \tag{3}$$

The timing chart in Eqs. (2) to (3) is shown in Fig. 3, which consists of MIMO channel estimation, preprocessing (matrix inversion), and MIMO detection. The channel estimation extracts the MIMO channel matrix of $\boldsymbol{H}_k$ from training symbols. The preprocessing calculates the inverted matrix of $\boldsymbol{G}_k$. The MIMO detection decodes the original data from the received signals in the data symbols. When a MIMO-OFDM receiver computes the inverted matrix of $\boldsymbol{G}_k$ and use it for the MIMO detection in the same packet, the preprocessing should finish by receiving the first data symbol.

The block diagram of a 8×8 MIMO detector is shown in Fig. 4. The input data in the MIMO detection block are given by the estimated MIMO channel matrix of $\boldsymbol{H}_k$ with k-th frequency bin and $M_T \times M_R$ matrix. The matrices of $\boldsymbol{P}_k$, $\boldsymbol{R}_k$, and $\boldsymbol{G}_k$ are computed as

$$\boldsymbol{P}_k = \boldsymbol{H}_k^H \boldsymbol{H}_k + \sigma^2 \boldsymbol{I} \tag{4}$$

$$\boldsymbol{Q}_k = \boldsymbol{H}_k^H \tag{5}$$

$$\boldsymbol{R}_k = \boldsymbol{P}_k^{-1} \tag{6}$$

$$\boldsymbol{G}_k = \boldsymbol{R}_k \boldsymbol{Q}_k, \tag{7}$$

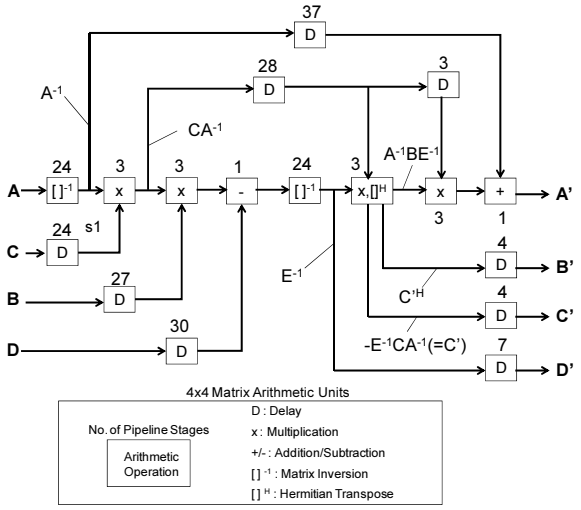

Fig.5: *Complete pipeline MIMO detector.*

Step	Equations	Number of Matrix Arithmetic Units		
		4x4 MUL	4x4 ADD	4x4 INV
#1	(12)	2	1	0
#2	(13)	2	1	0
#3	(14)	2	1	0
#4	(15) – (18)	2	1	1
#5	(19) – (22)	2	1	1
#6	(23)	2	1	0
#7	(24)	2	1	0
#8	(25)	2	1	0
#9	(26)	2	1	0

The output data of $\boldsymbol{G}_k$ are stored in the memory unit and retrieved in the MIMO decoding process. We use Strassen's algorithm for the matrix inversion, which divides a square matrix into four block matrices. For an 8×8 matrix $\boldsymbol{\Omega}$, it is divided into 4×4 block matrices as

$$\boldsymbol{\Omega} = \begin{pmatrix} \boldsymbol{A} & \boldsymbol{B} \\ \boldsymbol{C} & \boldsymbol{D} \end{pmatrix}, \tag{8}$$

where $\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}, \boldsymbol{D}$ are the 4×4 matrices. $\boldsymbol{\Omega^{-1}}$ is calculated by

$$\begin{aligned} \boldsymbol{\Omega}^{-1} &= \begin{pmatrix} \boldsymbol{F} & -\boldsymbol{A}^{-1}\boldsymbol{B}\boldsymbol{E}^{-1} \\ -\boldsymbol{E}^{-1}\boldsymbol{C}\boldsymbol{A}^{-1} & \boldsymbol{E}^{-1} \end{pmatrix} \\ &= \begin{pmatrix} \boldsymbol{A}' & \boldsymbol{B}' \\ \boldsymbol{C}' & \boldsymbol{D}' \end{pmatrix}, \end{aligned} \tag{9}$$

$$\boldsymbol{F} = \boldsymbol{A}^{-1} + \boldsymbol{A}^{-1}\boldsymbol{B}\boldsymbol{E}^{-1}\boldsymbol{C}\boldsymbol{A}^{-1} \tag{10}$$

$$\boldsymbol{E} = \boldsymbol{D} - \boldsymbol{C}\boldsymbol{A}^{-1}\boldsymbol{B}. \tag{11}$$

where $\boldsymbol{\Omega}$ is a Hermitian matrix composing $\boldsymbol{C} = \boldsymbol{B}^H, \boldsymbol{B}' = \boldsymbol{C}'^H$. This property gives the relation of $\boldsymbol{A}^{-1}\boldsymbol{B} = (\boldsymbol{C}\boldsymbol{A}^{-1})^H$. The calculation of $\boldsymbol{C}\boldsymbol{A}^{-1}$ can omit the calculation of $\boldsymbol{A}^{-1}\boldsymbol{B}$.

A complete pipeline MIMO detector is depicted in Fig. 5, which connects all 4x4 matrix units of matrix adder, subtractor, multiplier, and inversion units.

Table 2: *Implementation results of 8×8 MIMO detectors*

	Complete Pipeline	9-Step Computation
Wordlength (bits)	26	24
Logic Gate Count	15.4 M	2.3 M
Clock Frequency (MHz)	100	100
Pipeline Latency (μs)	0.78	9.63
Power Dissipation (mW)	1,420	230

The matrix inversion unit computes the Strassen's matrix inversion in Eqs. (9)-(11). The delay units are inserted for adjusting pipeline latency delays. This detector achieves the highest throughput performance by one data output per cycle, however needs considerable hardware. To reduce circuit scale, we present a 9-step pipeline MIMO detector which divides the whole computation into 9 steps. In case of the 9-step computation, Eqs. (4)-(7) can be divided by the following equations:

$$\boldsymbol{b}_{11} = \boldsymbol{h}_{11}\boldsymbol{h}_{11} + \boldsymbol{h}_{12}\boldsymbol{h}_{12}^* + \sigma^2\boldsymbol{I} \tag{12}$$

$$\boldsymbol{b}_{12} = \boldsymbol{h}_{11}\boldsymbol{h}_{21}^* + \boldsymbol{h}_{12}\boldsymbol{h}_{22} \tag{13}$$

$$\boldsymbol{b}_{22} = \boldsymbol{h}_{21}\boldsymbol{h}_{21}^* + \boldsymbol{h}_{22}\boldsymbol{h}_{22} + \sigma^2\boldsymbol{I} \tag{14}$$

$$\boldsymbol{c}_1 = \boldsymbol{b}_{11}^{-1} \tag{15}$$

$$\boldsymbol{c}_2 = \boldsymbol{b}_{12}^H\boldsymbol{c}_1 \tag{16}$$

$$\boldsymbol{c}_3 = \boldsymbol{c}_2\boldsymbol{b}_{12} \tag{17}$$

$$\boldsymbol{c}_4 = \boldsymbol{b}_{22} - \boldsymbol{c}_3 \tag{18}$$

$$\boldsymbol{c}_5 = \boldsymbol{c}_4^{-1} \tag{19}$$

$$\boldsymbol{c}_6 = \boldsymbol{c}_2^H\boldsymbol{c}_5 \tag{20}$$

$$\boldsymbol{c}_7 = \boldsymbol{c}_6\boldsymbol{c}_2 \tag{21}$$

$$\boldsymbol{c}_8 = \boldsymbol{c}_1 + \boldsymbol{c}_7 \tag{22}$$

$$\boldsymbol{g}_{11} = \boldsymbol{c}_8\boldsymbol{h}_{11} - \boldsymbol{c}_6\boldsymbol{h}_{21} \tag{23}$$

$$\boldsymbol{g}_{12} = \boldsymbol{c}_8\boldsymbol{h}_{12} - \boldsymbol{c}_6\boldsymbol{h}_{22} \tag{24}$$

$$\boldsymbol{g}_{21} = -\boldsymbol{c}_6^H\boldsymbol{h}_{11} + \boldsymbol{c}_5\boldsymbol{h}_{21} \tag{25}$$

$$\boldsymbol{g}_{22} = -\boldsymbol{c}_6^H\boldsymbol{h}_{12} + \boldsymbol{c}_5\boldsymbol{h}_{22}, \tag{26}$$

where $\boldsymbol{h}_{ij}$ and $\boldsymbol{g}_{ij}$ are 4x4 block matrices of $\boldsymbol{H}_k$ and $\boldsymbol{G}_k$, respectively. These equations are computed by 4x4 matrices operations. The division of 9-step computations in Strassen's algorithm is shown in Table 1. Eqs. (12)-(26) are divided so as to equalize the numbers of matrix operations (multiplication, addition/subtraction, and inversion) at each step. The minimum requirement of 4x4 matrix arithmetic units in circuit design is given by this division, i.e., two multiplication units, one addition/subtraction unit, and one inversion unit. The circuit structure of the 9-step pipeline detector is illustrated in Fig. 6. The signal input of "Sel" is used for changing data paths in the matrix arithmetic units where different matrix operations can be executed in this dynamic reconfigurable architecture.

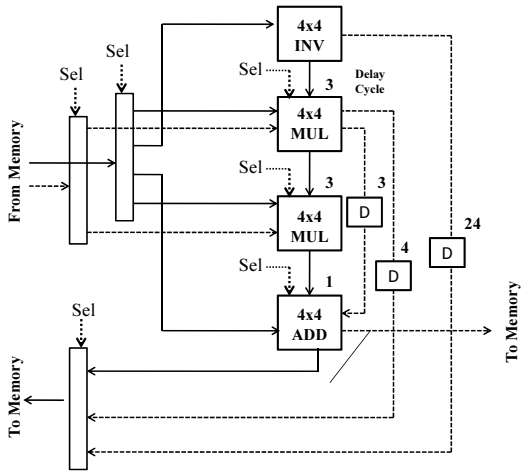

Fig.6: *9-step pipeline MIMO detector.*

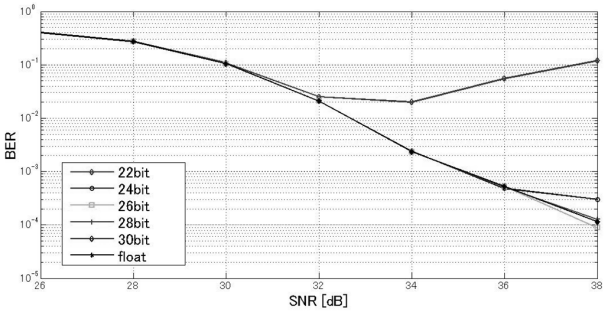

Fig.7: *Wordlength determination in complete pipeline detector.*

2.4 Implementation

The 8x8 MIMO detectors were implemented on a 90-nm CMOS technology, where a clock frequency was set to 100 MHz with 1.0-V supply voltage. The wordlengths of the MIMO detectors were determined by fixed-point simulation. Fig. 7 shows BER performance in the fixed-point (between 22 and 30 bits) and the floating-point (32 bits) operations. The wordlengths of the detector were set to 26 bits in the fixed-point precision. The implementation results of the MIMO detectors is summarized in Table 2. The complete pipeline detector shows low latency and a large circuit. The 9-step pipeline detector has a small circuit and long latency. For high mobility in wireless terminals assuming that a receiver must decode MIMO signals within one packet period (i.e., fast fading environments), the complete pipeline detector is desirable. For moderate mobility assumed in WLAN applications, the 9-step pipeline detector is enough for real-time processing in MIMO detection.

The whole implementation result of the 8×8 MIMO-OFDM transceiver is summarized in Table 3. The 9-step pipeline MIMO detector has been adopted in the MIMO detection block. Since the other blocks has been developed in our previous works [7] and [8],

Table 3: *Implementation result of 8×8 MIMO-OFDM transceiver.*

Transmitter	Logic Gate Count	Power Dissipation (mW)
Scramble	4,830	0.57
Encoding	5,390	0.60
Interleave	104,020	14.2
Mapping	5,480	0.52
Pilot Insertion	218,970	29.9
IFFT	573,680	57.9
GI & Preamble Insertion	330,720	44.5
Total	1,243,090	148.2

Receiver	Logic Gate Count	Power Dissipation (mW)
Synchronization	21,410	2.5
FFT	573,920	81.0
Re-order & Pilot Removal	235,370	33.4
Channel Estimation & MIMO Detection	7,800,630	956.6
De-mapping	14,580	1.1
De-interleave	676,930	73.4
Viterbi Decoding	2,711,330	257.6
De-Scramble	4,830	0.30
Total	12,039,000	1,405.9

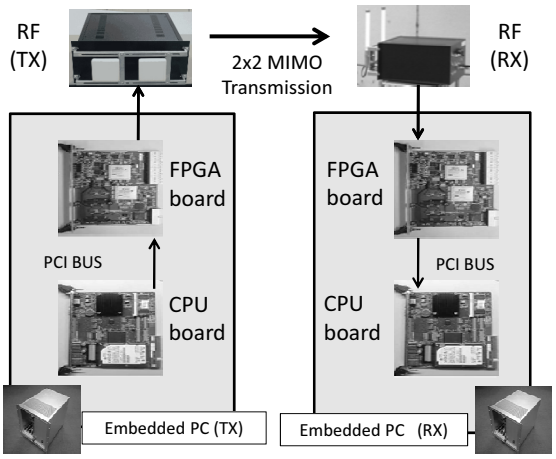

Fig.8: *Structure of MIMO-OFDM testbed.*

the explanation of their circuit structures is omitted. The power dissipation was 1.41 W in the receiver and the gate count was 13.3 millions in both the transmitter and receiver. The MIMO detection block was the most costly in terms of both circuit area and power dissipation. Compared with the 4×4 MIMO-OFDM transceiver developed in our work [7], circuit area and power dissipation increase threefold.

3. MIMO-OFDM TESTBED

3.1 Structure

The 2x2 MIMO-OFDM testbed we developed is illustrated in Fig. 8. The baseband unit consists of the FPGA and CPU boards. In the CPU board, an embedded PC provides the monitor display and network connection. The FPGA board is controlled by the commands sent from the CPU board. We

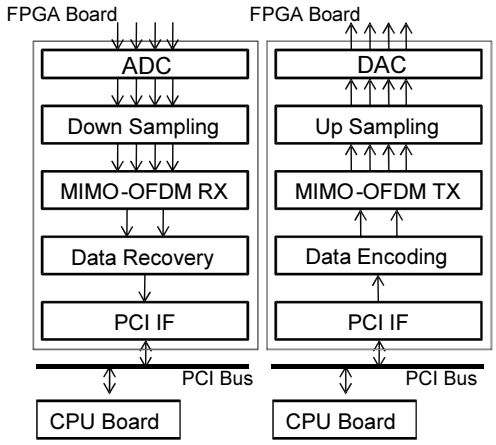

Fig.9: *Block diagram of transmitter and receiver in FPGA board.*

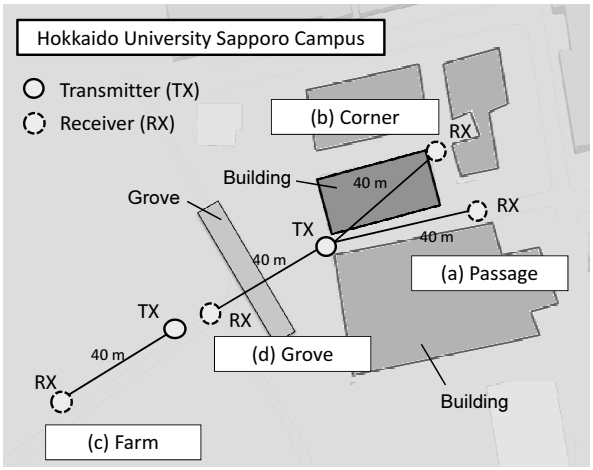

Fig.10: *Experimental location.*

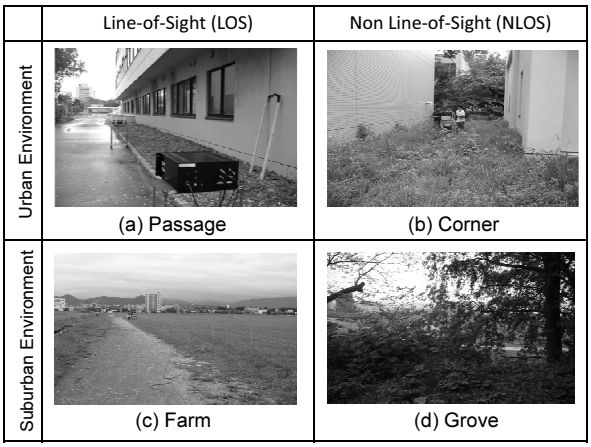

Fig.11: *Experimental environments.*

Table 4: *Experimental conditions*

Radio Frequency Band	5150 - 5250 MHz
Transmit Power per Antenna	14 dBm
TX Antenna (Directional)	NATEC PAT509S-4953 9 dBi / E-Plane 58 deg / H-Plane 76 deg
RX Antenna (Directional)	NATEC VA505A-W52 5 dBi / E-Plane 40 deg / H-Plane 360 deg
Sampling Rate in DAC/ADC	400 Msps
Communication System	2x2 MIMO-OFDM
Transmitted Signal Bandwidth	79.68 MHz
Modulation & Coding	QPSK, 16QAM
Coding	Convolutional Coding (Coding Rate 1/2)
Error Correcting	Viterbi Decoding

have developed a GUI-based measurement software on this computer platform to evaluate the communication performance and propagation channel characteristics during the field experiment. The measurement software provides the signals monitoring and BER, PER, and QAM constellation measurements. The baseband signals in the FPGA board are inputted into the DAC modules and outputted from the ADC modules. The RF unit is designed based on super heterodyne architecture where the signals are modulated/demodulated at 5200 MHz and 374 MHz in the RF and intermediate frequency (IF) bands, respectively. The details of RF transceiver has been explained in [9].

A block diagram of the FPGA board is illustrated in Fig. 9. The transmitted data sent from the CPU board are encoded and converted into MIMO-OFDM signals in the "Data Encoding" and "MIMO-OFDM TX", respectively. "Up Sampling" block executes low pass filtering. DAC/ADC module operates in 200MHz clock frequency with a double-data-rate (DDR) of 400 Msps sampling frequency. The signals in the up-sampling unit are interpolated and filtered by the low-pass FIR filter. We used a Xilinx Virtex-5 XC5VLX330T FPGA device in the FPGA implementation. The 2x2 MIMO-OFDM transceiver has 14 bits in the input/output ports with a maximum 20 bits in the arithmetic operations. The result of a maximum clock frequency is 108 MHz. The total percentage of FPGA utilization is at most about 32 % at most.

3.2 Field Experiment

We evaluated communication performance using our testbed in outdoor environments. The experimental location and environments are shown in Fig. 10 and Fig. 11, respectively. The field experiment was performed in the Hokkaido University Sapporo Campus. We evaluated four environments of "passage", "corner", "farm", and "grove" which are classified into LOS or NLOS and urban or suburban conditions. The experimental conditions are enumerated in Table 4. We tested QPSK and 16QAM with an 1/2-coding rate in modulation, whose modulation modes correspond to 133 and 266 Mbps data rates in the PHY layer, respectively. The maximum transmit power per antenna was set to 14 dBm.

The experimental results of throughput, measured SNR, eigenvalue gap, channel capacity are summa-

Table 5: *Experimental results*

Environment	(a) Passage	(b) Corner	(c) Farm	(d) Grove
Area	Urban	Urban	Suburban	Suburban
Line-of-Sight Condition	LOS	NLOS	LOS	NLOS
Maximum Throughput (Mbps)	266.0	125.0	101.1	143.6
Measured SNR (dB)	32.9	23.3	33.6	26.4
Eigenvalue Gap between λ_1 and λ_2 (dB)	11.7	10.2	26.5	11.5
Channel Capacity (bps/Hz)	8.76	7.10	7.55	5.43

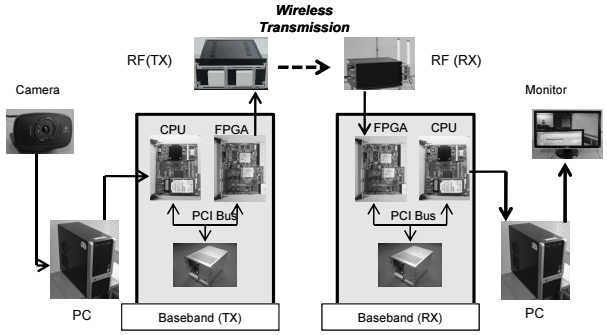

Fig.12: *Structure of video transmission equipment.*

rized in Table 5. The measured SNR is given by a ratio of the measured signal power and noise power. The channel capacity can be calculated from the MIMO channel matrix and SNR value [10]. We use the following equation for this:

$$C = E\Big[\frac{1}{K}\sum_{k=1}^{K}\log_2\Big(\det(\boldsymbol{I} + \frac{P}{\sigma^2}\boldsymbol{H}_k\boldsymbol{H}_k^H)\Big)\Big], \tag{27}$$

where $\boldsymbol{H}_k$ is the MIMO channel matrix with a k-th subcarrier matrix. P and σ^2 denote the received signal power and noise variance, respectively. K is the number of data subcarriers. The channel capacity assumes ideal MIMO communication and is not suited to evaluate actual throughput in the testbed. Hence, the results of maximum throughput do not accord to those of channel capacity. The passage environment shows the best performance in maximum throughout due to the high SNR and the low eigenvalue gap values. The farm environment presents the high SNR value as much as the passage environments. However, it decreases throughput because the low eigenvalue gap makes MIMO signal separation difficult. Our experiment showed that the farm environment is the severest in outdoor MIMO communication.

3.3 Video Transmission Equipment

The wireless video transmission equipment is illustrated in Fig. 12. Video encoding and decoding are executed by software on PCs. VLC Media Player is used for packet data streaming and specifies a specified IP address with a port number . It can also

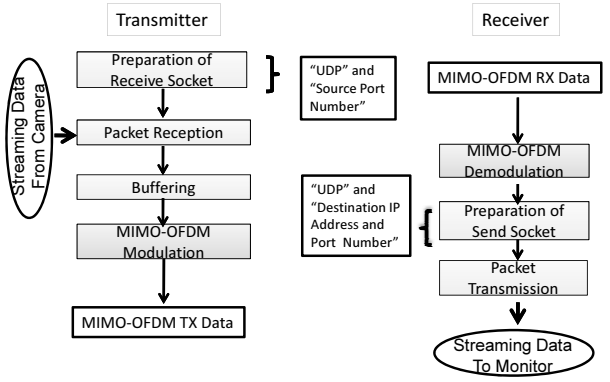

Fig.13: *Procedure of streaming data relay program.*

change a video format and a data rate in video encoding. In the transmitter side, the data captured in USB camera are transferred to PC. The packet data are generated and sent to the CPU board. The CPU board receives packet data and inserts a sequence number for each packet. The FPGA board converts packet data to baseband signals and sends to the RF unit after MIMO-OFDM modulation. The RF unit transmits RF signals by two transmitter antennas. In the receiver side, the FPGA board demodulates the MIMO signals and restores packet data in the CPU board. The CPU board removes the sequence number from packet data and sent to PC. Finally, the monitor displays camera pictures.

We have developed a program which relays streaming data on the CPU boards. Fig. 13 shows the procedure of the relay program. This program sends and receives streaming data by using Winsock application programming interface (API). The reception socket is prepared to receive packet data from PC in the transmitter side where the port number and the settings of reception in UDP are determined. The packet size of 1,316 bytes is defined as the specification of VLC Media Player. The reception socket receives streaming data until the buffer is full. Four types of packet numbers (1,3,6, and 12 packets) have been tested in the data buffering. The sequence number is added at the head of packet data. These data are sent to the FPGA board. The above procedure repeats for every packets. In the receiver side, the demodulated data from FPGA board are read out and the sequence number are removed. Destination port number, IP address, and UDP parameters are assigned in the transmission socket.

We tested video quality of this equipment by changing the number of packets in the data buffering. The maximum video size was set to 1280×960 with MPEG4 encoding. We found that burring 6 packets shows the best quality due to low processing latency in the CPU board. Larger video sizes such as full HD will be tested after improvement of the relay program.

4. CONCLUSION

This paper describes hardware development of an 8×8 MIMO-OFDM baseband transceiver compatible with the IEEE802.11ac specification and 2×2 MIMO-OFDM FPGA-based testbed. The 8×8 MIMO-OFDM transceiver reaches 3 Gbps in the PHY layer. The two pipeline MMSE MIMO detector havw been designed for real-time processing in MIMO detection. We have prototyped the 2×2 MIMO-OFDM testbed for field experiment and video transmission. The field experiment showed that the maximum throughout strongly depends on MIMO environments. The video transmission equipment provides real-time video transmission by relaying streaming packets. The development of 4×4 and 8×8 MIMO-OFDM testbeds remain to done in our future work.

5. ACKNOWLEDGMENT

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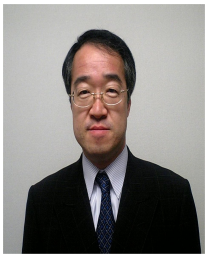

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