Design and Modeling of Highly Power efficient Node-level DC UPS

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ABSTRACT

This paper presents design and modeling of a highly efficient node-level DC uninterruptible power supply (UPS) in rack-level DC power architecture. In the previous research, we proposed the architecture of the highly efficient rack-level DC system combined with node-level DC UPS. This paper deals with the design and modeling of proposed node-level DC UPS.

Keywords: Rack-level DC Power Supply, Power Monitoring, Node-level DC UPS, Power Distribution

1. INTRODUCTION

Energy efficiency is the most important part in the data center evaluation. As the Google's and Facebook server farm, low cost x86 platform-based servers have been extensively used in search and cluster fields. Green Grid Association is working to provide industry-wide recommendations and best practices on metrics and technologies that will improve energy efficiency in data centers [1].

Research on changing existing AC data centers to DC data centers as a means to improve power efficiency is actively in progress. Google has changed to a +12 V single DC power supply to improve energy efficiency [2]. Lawrence Berkeley National Laboratory teamed with about 20 companies to demonstrate that using DC entirely throughout a data center will save 10% to 20% in power costs and improve reliability [3], [4]. Nevertheless, DC power distribution makes sense if a company is building a petabyte-scale data center from the ground up. There are many problems, such as compatibility with existing computer equipment and cable standardizations [5]. Some blade systems support DC distribution using dynamic load-sharing methods to improve power efficiency [6]. However, these blade systems are expensive and do not provide compatibility with low-cost commodity volume servers or PC system power.

To solve the problems, we have studied out rack-level DC power distribution system for the data center in some papers [6], [7]. The first paper proposed the rack power supply unit (RPSU), a rack-level smart DC rectifier, which is fully compatible with existing data center power infrastructures, racks, and servers. The RPSU system can solve power problems in a volume server, such as low-power efficiency, no power redundancy, and no power monitoring. The measurement results of the RPSU system show over a 10% power efficiency improvement compared to an AC system providing N+1 redundant power. Moreover, the power information of the RPSU system can be monitored through a network.

The second paper proposed a 12 V rack-level DC rectifier combined with a node-level DC UPS (uPDB). The proposed uPDB reduces conversion loss by including a DC UPS, and increases efficiency using a 12 V bypass architecture.

In this paper, we deal with proposed uPDB hardware design and power modeling. And we will make power modeling equation for node-level DC UPS system include rack-level DC power supply.

2. NEW POWER DELIVERY ARCHITECTURE

Existing power delivery is divided into three broad categories: AC, rack-level DC, and facility-level DC. In a conventional AC power delivery architecture, the UPS, power distribution unit (PDU), and PSU power make up the delivery path. In the delivery path, double conversion, AC/DC or DC/DC, occurs at the UPS and PSU, causing power loss. On the other hand, facility-level DC power distribution provides 48 V or 400 V DC prior to the UPS, reducing AC/DC power conversion loss at the UPS and PSU, improving the overall efficiency. A rack-level DC delivery architecture using a highly efficient rectifier provides 48 V or 400 V DC power in the rack and the PDB changes to 12 V DC power at the server in Fig. 2. Since the number of conversion stages is the same as in AC architectures, a simply reorganized rack-level DC cannot improve efficiency, and simply provides rack-level power redundancy [8].

In previous paper, we proposed highly-efficient rack-level DC power architecture combined with a node-level DC UPS, as shown in Fig. 2. First, we remove the facility-level UPS located in front of the PDU and make a node-level DC UPS, which improves the efficiency of the UPS by reducing energy conversion instantly and distributing the UPS at the node-level. Second, we used a 12 V rack-level RPSU with

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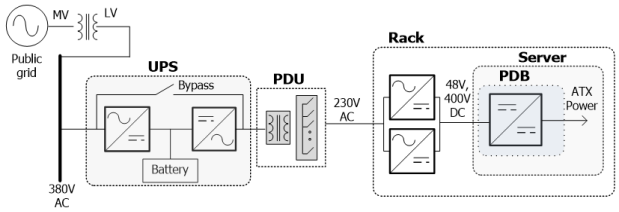

Fig.1: *General rack-level DC power distribution architecture.*

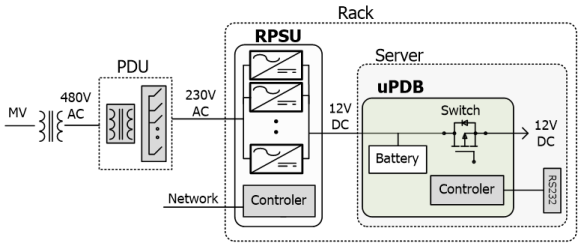

Fig.2: *Rack-level DC power distribution architecture combined with node-level DC UPS.*

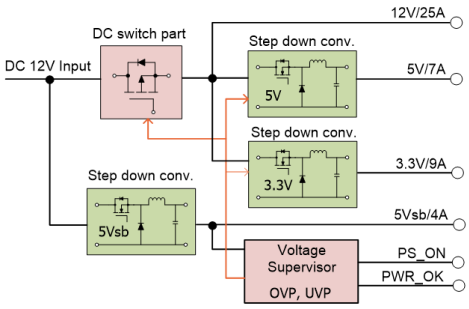

Fig.3: *PDB block diagram.*

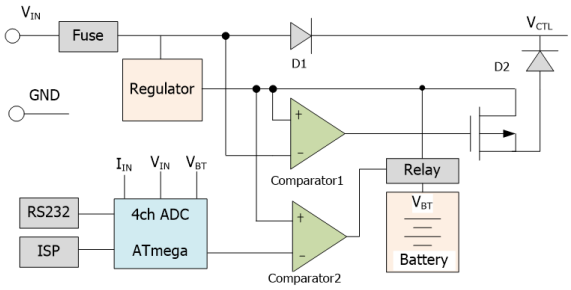

Fig.4: *uPDB battery control block diagram and design picture.*

DC power supply consisting of multipower modules and supporting a dynamic load-sharing method that automatically turns on/off the multipower modules optimally based on the load amount.

Therefore, the RPSU supports more efficient power at low loads providing N+1 power redundancy. Third, we reduce DC/DC conversion loss by making a 12 V bypass PDB, which provides 12 V directly to the motherboard without any DC/DC conversion in previous research.

3. DESIGN OF UPDB

uPDB is mainly consist of PDB and battery controller. First, we deal with PDB design. The PDB generates ATX compatible power from 12 V single DC supplied from the RPSU. Considering the PDB efficiency and cost, this paper proposes a method that uses 12 V directly to ATX power from the RPSU without any conversion.

A hardware block diagram of the PDB is shown in Fig. 3. If 12 V power is input into the PDB, the PDB first generates 5 Vsb using a step-down converter. The 5 Vsb provides power for server standby and the voltage supervisor chip of the PDB. The voltage supervisor chip controls a 12 V bypass switch and step-down converter of 3.3 V or 5 V when PS_ON is inputted. If the output of 3.3 V or 5 V has a problem, the voltage supervisor chip also has over-voltage protection and under-voltage protection functions. If all of output voltages are valid, the PDB generates a PWR_OK signal for the motherboard. All signals generated from the PDB are compatible with ATX power specifications. The PDB can optionally support node current and voltage sensing using an ADC, and this sensing information is transferred to the host server or PC agent software through RS232. The PDB is designed with maximum 20 A current, and can therefore provide up to 240 W of power. The output specifications of PDB are 12 V/20 A, 5 V/7 A, 3.3 V/9 A, and 5 Vsb/4 A.

Figure 4 shows uPDB controller block diagram. The 12 V power goes through D1 diode and supply power PDB in normal operation. The uPDB controls the relay by detecting battery voltage (VBT). If input voltage (VIN) happens to fail, D1 diode short by comparator activate.

The micro-controller attached uPDB controls UPS operation and sends information of UPS states through RS232 interface to host agent. Each uPDB agent sends gathered data to RPSU power management server. The size of the uPDB is a small form factor of 15 cm×8 cm. Thus, it can be installed in any volume server or PC in place of a PSU. It is used serial connected eleven Ni-NH battery, 1.2 V and 4500 mA. It can cover twenty minutes backup time in experiment using HP DL320G5 server in table 1.

4. MODELING OF UPDB

The uPDB can be modeling base on PDB test result. The PDB is better power efficiency designed with 12 V bypass architecture. Fig. 5 shows ATX power consumption in general volume server or PC. The 12 V power consumption changes in proportion to load the other hand 3.3 V and 5 V power consumption do not change to the load.

The power efficiency of the PDB is the sum of the

output powers divided by the input power. It can be defined as

$$Eff_{PDB} = \frac{\sum_i P_{0,i}}{P_{in}} = \frac{P_{12V} + P_{5V} + P_{3.3V}}{P_{in}} \quad (1)$$

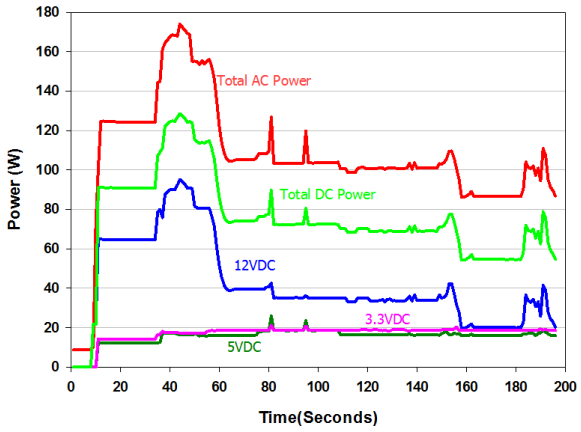

Fig.5: *ATX power consumption of volume server or PC.*

where P_{in} is the input DC power, P_{12V} is the output power at 12 V, P5 V is the output power at 5 V, and $P_{3.3V}$ is the output power at 3.3 V.

An HP DL320G5 server was used in the experiment, as detailed in Table 1. The PDB at 12 V can be replaced after removing the local PSU in a server. Table 2 shows the measured values of Pin, P_{12V}, P_{5V}, and $P_{3.3V}$ for a server in an idle state taken using a power meter and ATX cable jig. The measured power efficiency of the PDB at 12 V was 93.5% in an idle state.

The load-efficiency of each voltage in the PDB can be measured by connecting an electronic loader for each load and changing its values while simultaneously measuring the input power. Figure 9 shows the measurement results. Consider the results of PDB at 12 V. As the load increases, the power efficiency of 12 V almost reaches 100% since PDB at 12 V uses 12 V power directly from the RPSU. For 5 V, it reaches 89% maximum efficiency, while 3.3 V reaches 86%.

Table 1: *Cloud Computing Instance Costs.*

Unit	Specification
Processor	Intel Xeon QuardCore 3200
Memory	DDR2 2G ECC
HDD	500G SATA
Management	iLO2
PSU / Capacity	Delta DPS-400AB-1 / 450 W

We modeled the PDB on the description in section V. Since the PDB is designed with 12 V bypass architecture, the power efficiency of 12 V is better than 3.3 V or 5 V. Therefore, the PDB has its lowest

Table 2: *Cloud Computing Instance Costs.*

Item	PDB(Watt)	uPDB(Watt)
P_{in}	56.0	57.52
P_{12V}	17.7	
P_{5V}	16.1	
$P_{3.3V}$	18.6	
Efficiency	93.5%	91.1%

power efficiency in an idle state, which has the lowest 12 V power consumption of any computer operation. As computer load increases, the 12 V power of the PDB linearly increases. However, the 3.3 V and 5 V powers hardly change with load in a volume server or PC as fig. 5. Therefore, as the PDB load increases, the efficiency of the PDB also linearly increases. Using linear modeling, the PDB power efficiency can be expressed as

$$Eff_{PDB} = a + b \times (I - I_a), \quad (2)$$

where a is the PDB efficiency in an idle state, b is the gradient, I is the current, and I_a is the idle current.

An HPDL320G5 server with specifications as shown in Table 1 was used in an experiment of the PDB power efficiency. Table 2 shows the experiment results: I_a is 4.7 A ($I_a = P_{in}/12$ V) and a is 93.5 %. Supposing that the power efficiency of the PDB converges to 99 % when the load current passes over 20 A, the coefficient b in (6) can be solved by using two points, (4.7 A, 93.5 %) and (20 A, 99%). The power efficiency of the PDB can finally be expressed as

$$Eff_{PDB12V} = 93.5 + 0.36 \times (I - 4.7) = 0.36I + 9.18. \quad (3)$$

For modeling uPDB efficiency, considering UPS circuit loss. The loss of uPDB is the power loss cause to forward diode voltage drop and UPS control circuits. The loss of the forward diode happens at schottky diode, D1 in fig. 4.

Figure 5 shows schottky diode (S40HC1R5) forward current, IF according to forward voltage, VF. The power consumption of uPDB is 57.52 W at idle state in table 2. It is 1.52 W higher than PDB idle power consumption and the efficiency is 91.1%. Idle state current is 4.7 A and forward voltage VF=0.26V in typical case, UPS controller power consumption, PuPDB_ctrl can be solved 0.3W as (4)

$$P_{uPDB\_ctrl} = 1.52W - 4.7A \times 0.26V = 0.3W \quad (4)$$

The power consumption of D1 diode can be solved at 10 A and 20 A loads in the same way.

- VF=0.3V (Typical): 10A × 0.3V + 0.3W= 3.3W at 10A load
- VF=0.35V (Typical): 20A × 0.35V + 0.3W= 7.3W at 20A load

It can be applied linear modeling method to uPDB just like PDB modeling. PDB efficiency is 95.4 % at 10 A load in equation (3). uPDB consume over 3.3 W than PDB. Therefore uPDB efficiency is 92.85 % at 10 A load. Idle state (4.7 A, 91.1%) and 10 A load (10 A, 92.85 %). uPDB equation can be simplified as (5). uPDB efficiency down about 2.4 % and 2.8 % at idle and maximum load state each.

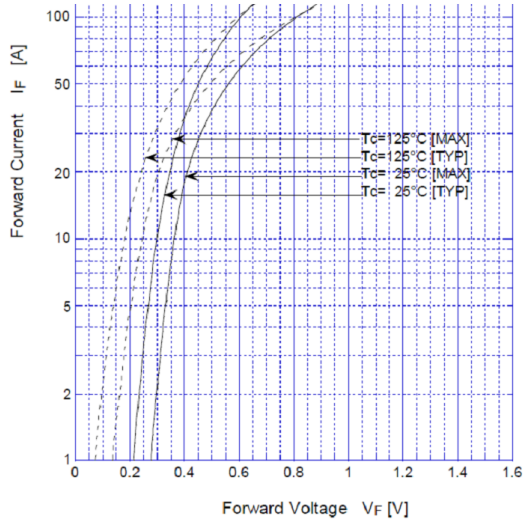

Fig.6: *Schottky diode (S40HC1R5) forward voltage as current in uPDB.*

$$Eff_{uPDB} = 91.1 + 0.33 \times (I - 4.7) = 0.33I + 89.55 \quad (5)$$

5. CONCLUSION

In this paper, we deal with design and power modeling of a proposed node-level DC UPS, uPDB proposed previous research. Designed uPDB has high power efficiency from 91.1% to 96% using 12 V bypass architecture and combined UPS. We extract power equation from uPDB using two points linear equation. Abstracted equation for uPDB can be used in power modeling at rack-level DC power system and can be comparing to another systems. Base on this research, we will make full system power equation and will analysis the efficiency in the future.

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